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MS-7510

Version : 1.0 *Diamond Edition*

CPU :

Intel Wolfield Family and Yorkfield Family Processor
Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 and 500 Sequence

System Chipset :

nVidia C72XE [C55 + BR04]
nVidia MCP55P

On Board Chipset :

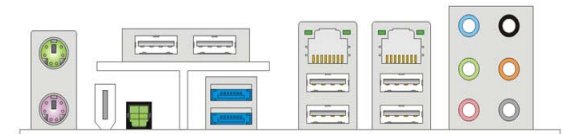
Azalia Codec -- RealTek ALC888
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 -- Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

Expansion Slot :

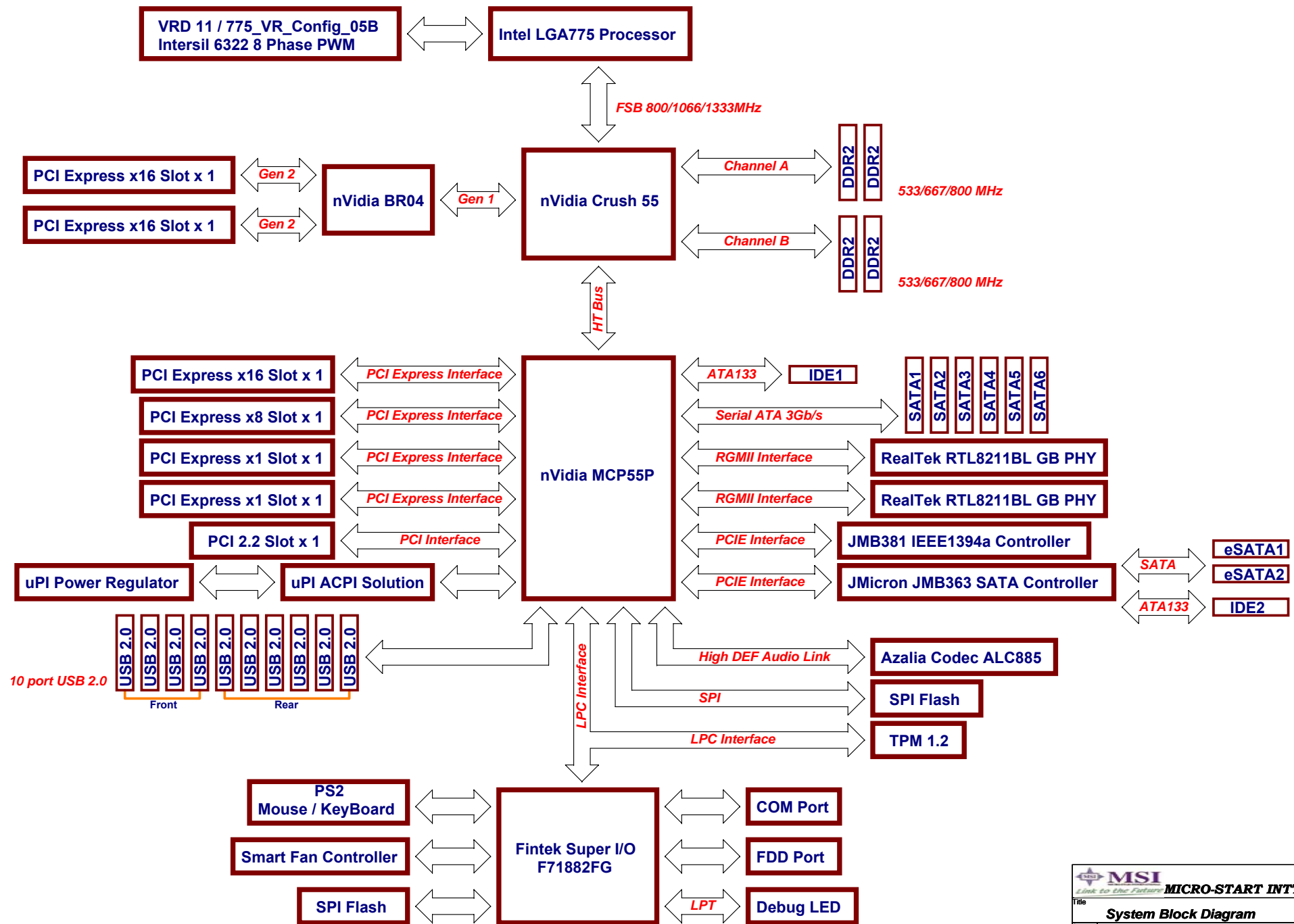
PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1



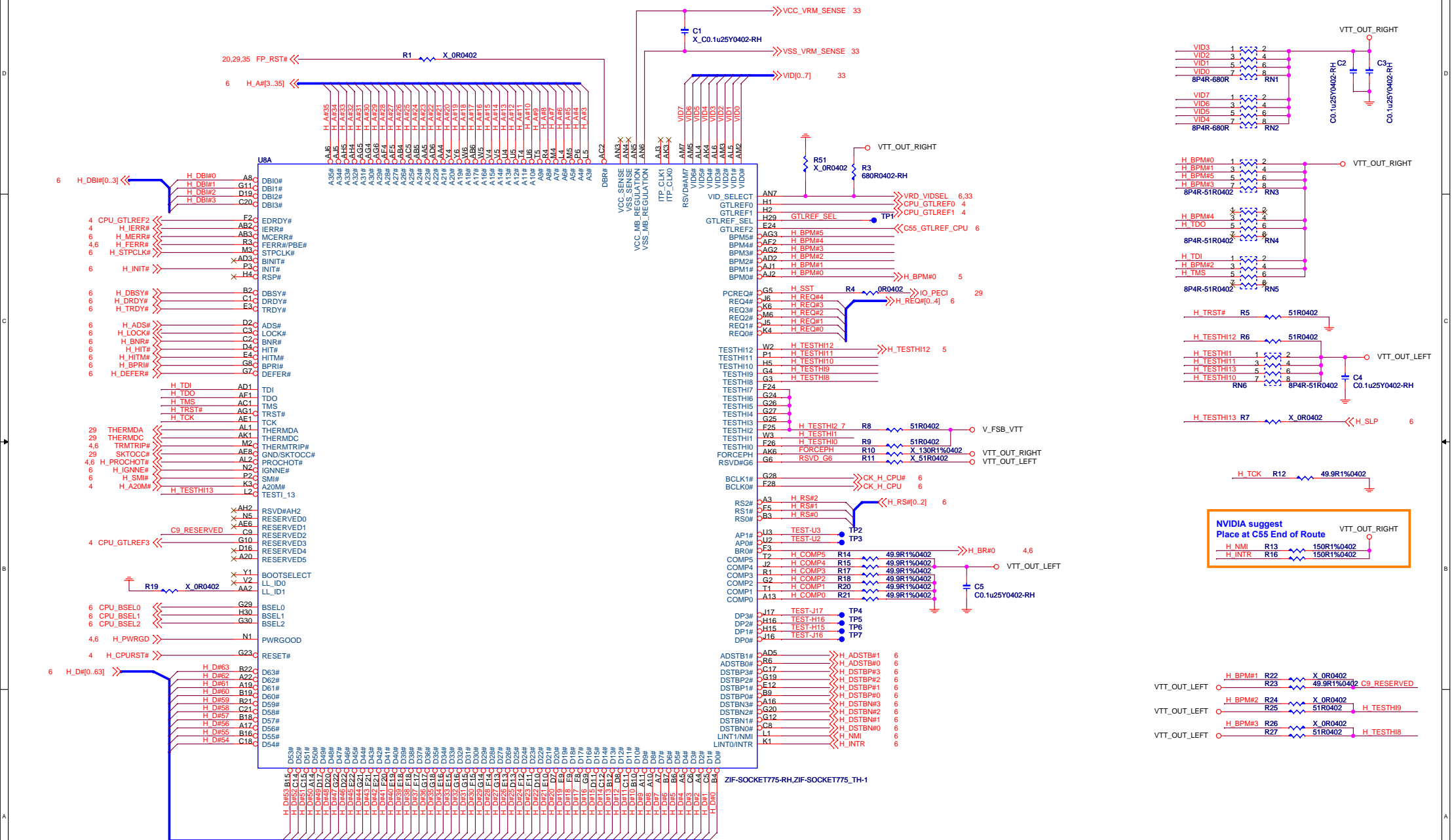
ERP No.	Config Item	PlatForm or Option	Option Select
7510-01S	Cfg-STD	C55 + BR04 + MCP55P + ALC888 + RTL8211BP + JMB381 + JMB363 + F71882FG	STD

MICRO-STAR INT'L CO.,LTD.		
Title Cover Sheet		
Size	Document Number	Rev
	MS-7510	1.0
Date: Tuesday, November 13, 2007	Sheet 1	of 41

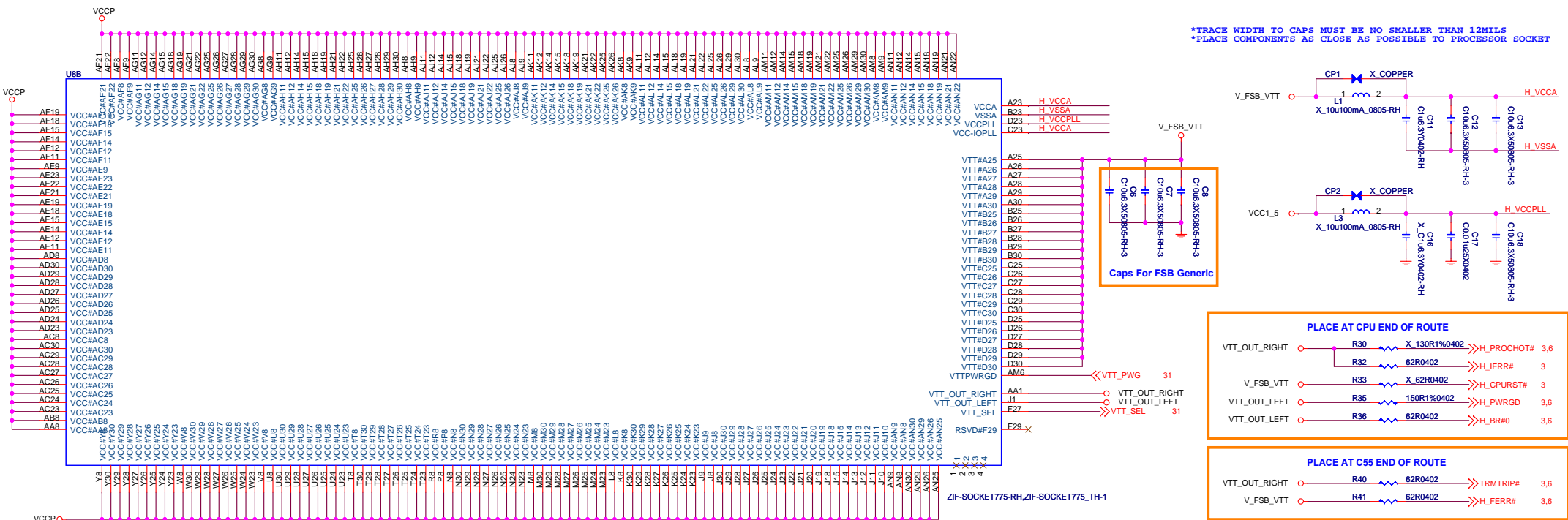
System Block Diagram



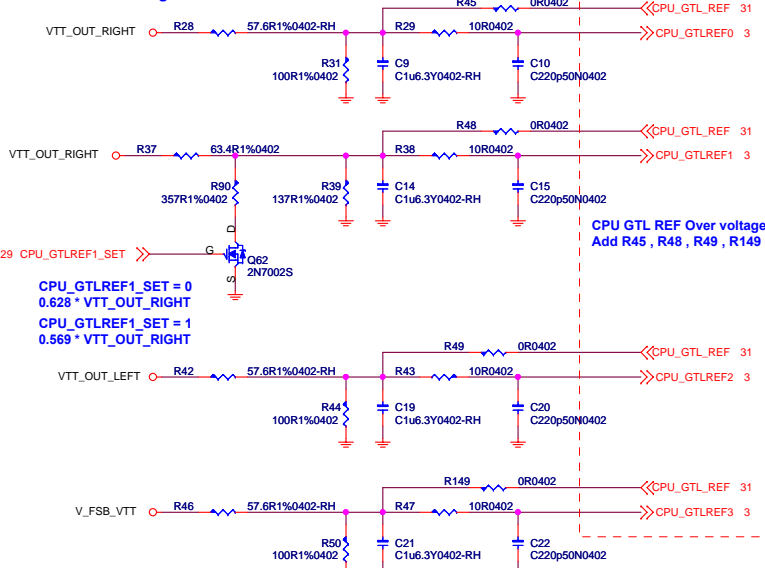
CPU LGA775 - Signals



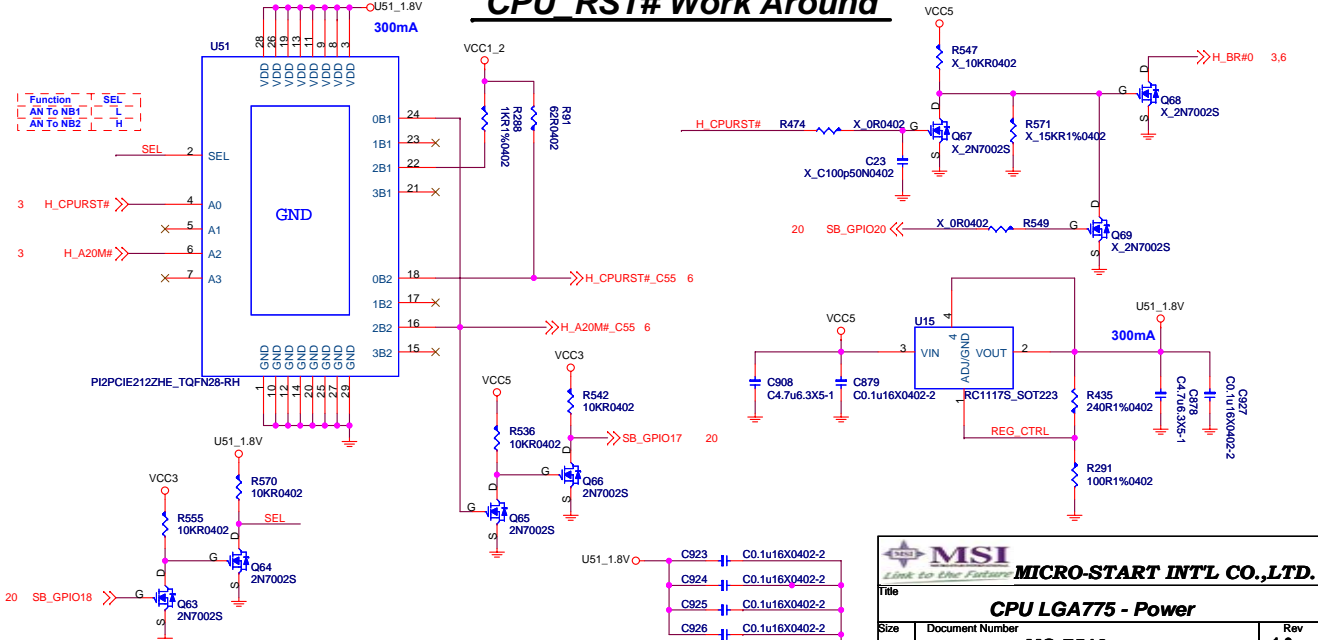
CPU LGA775 - Power



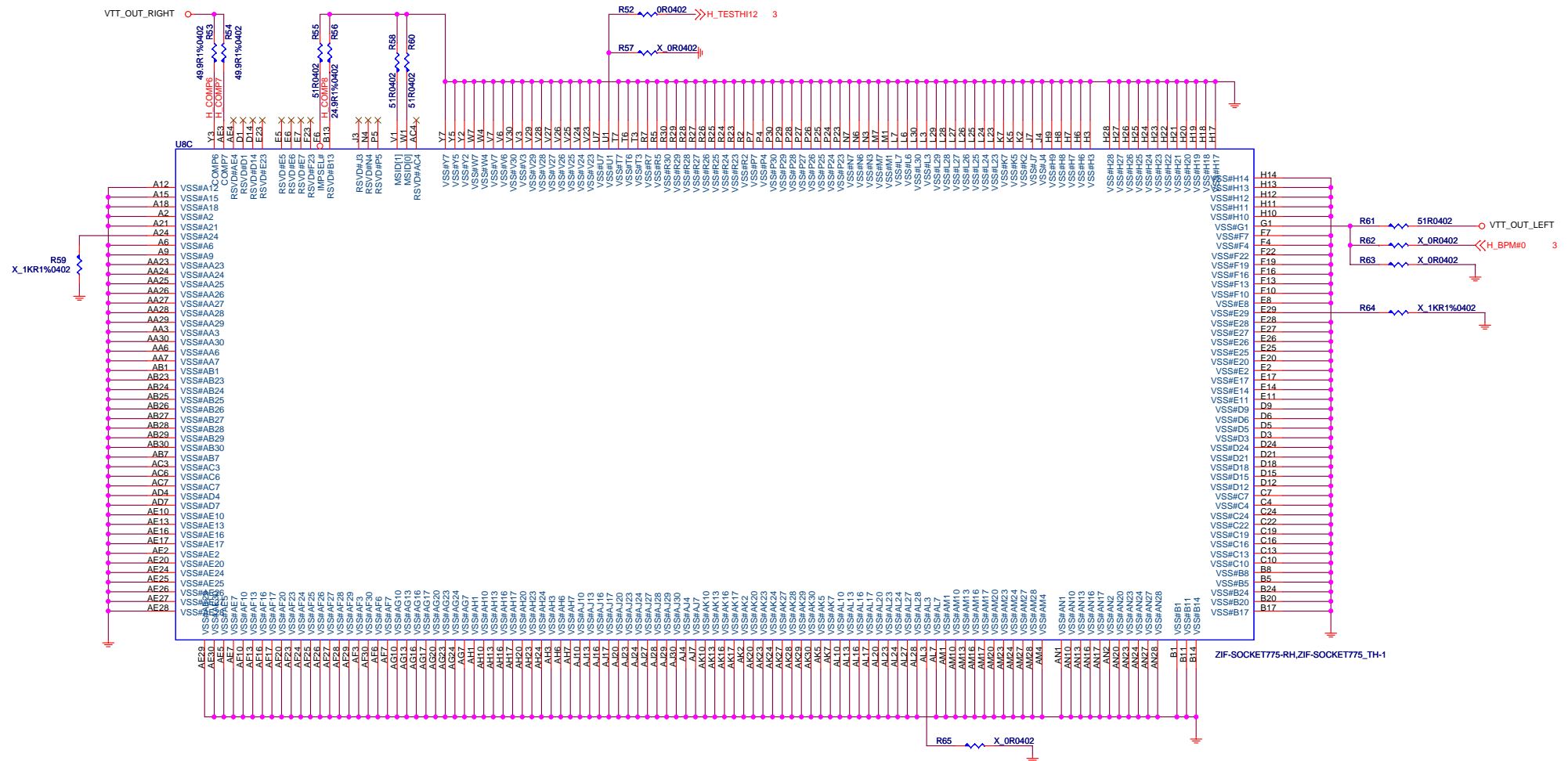
CPU GTLREF Voltage Should be 0.628 x VTT



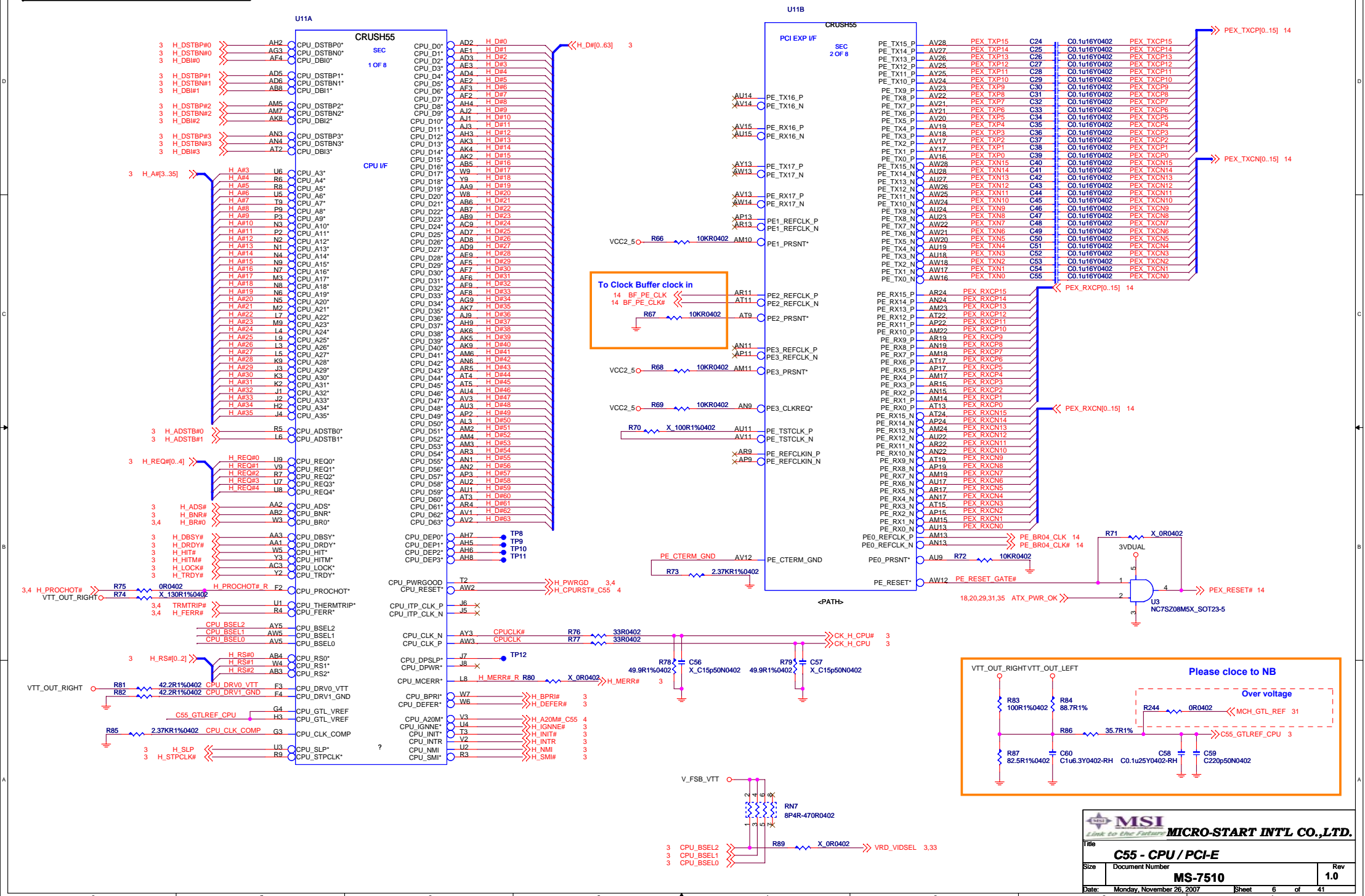
CPU RST# Work Around



CPU LGA775 - Gnd

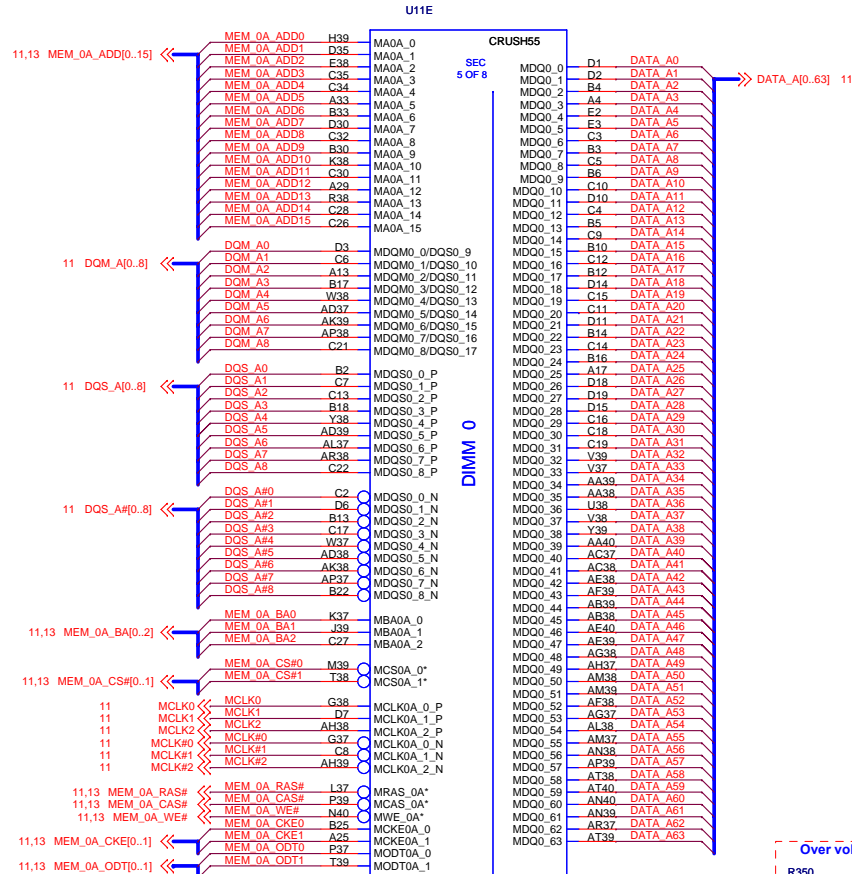


C55 - CPU / PCI-E

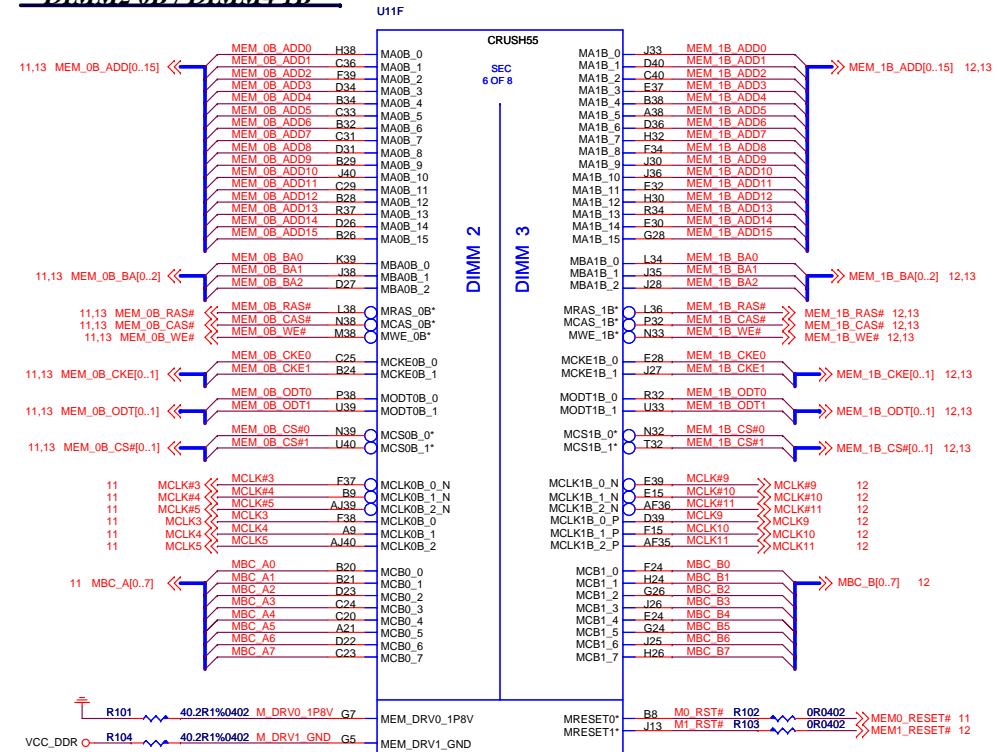


C55 - Memory A0

DIMM1 0A

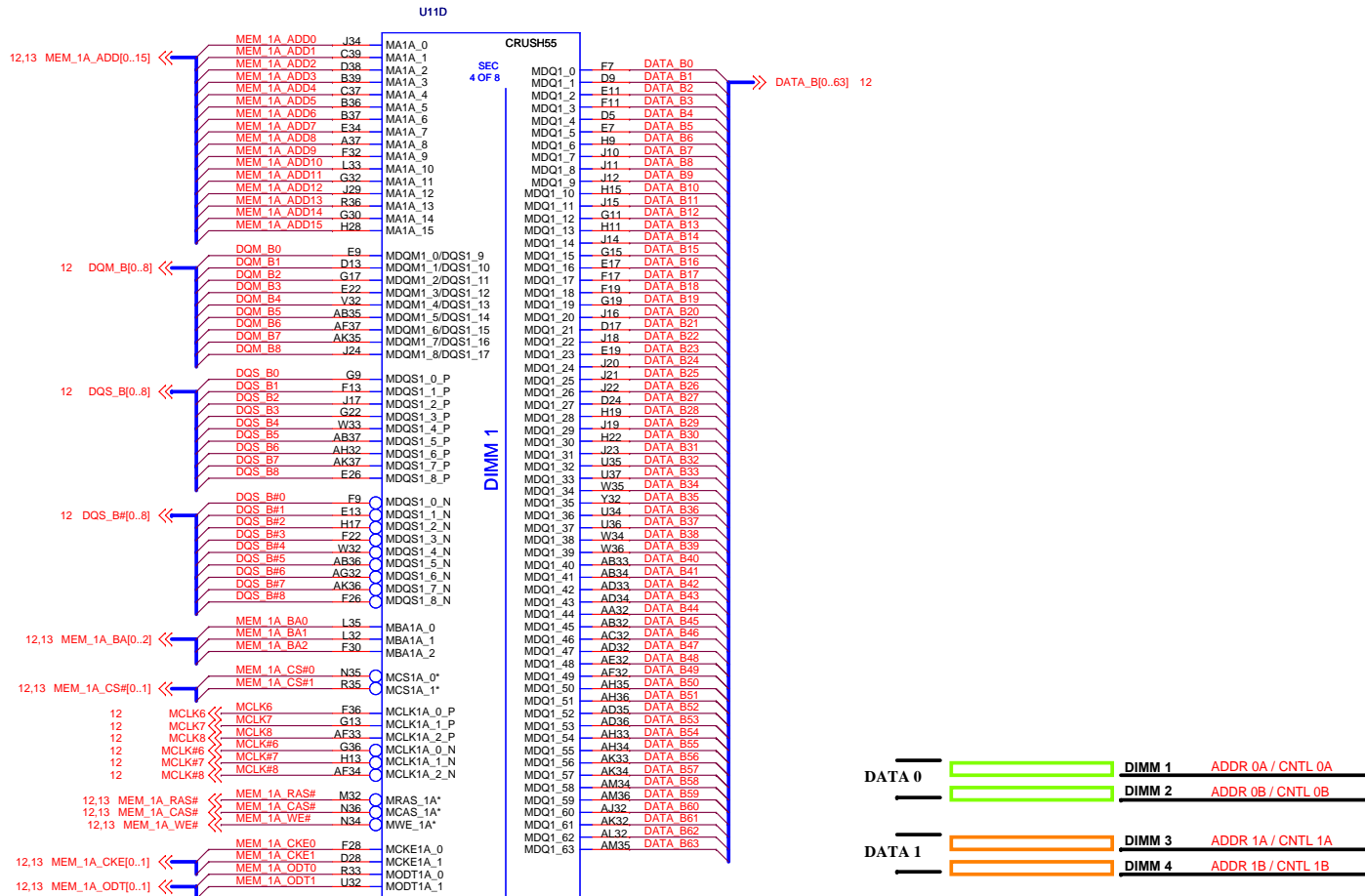


DIMM2 0B / DIMM4 1B



C55 - Memory A1

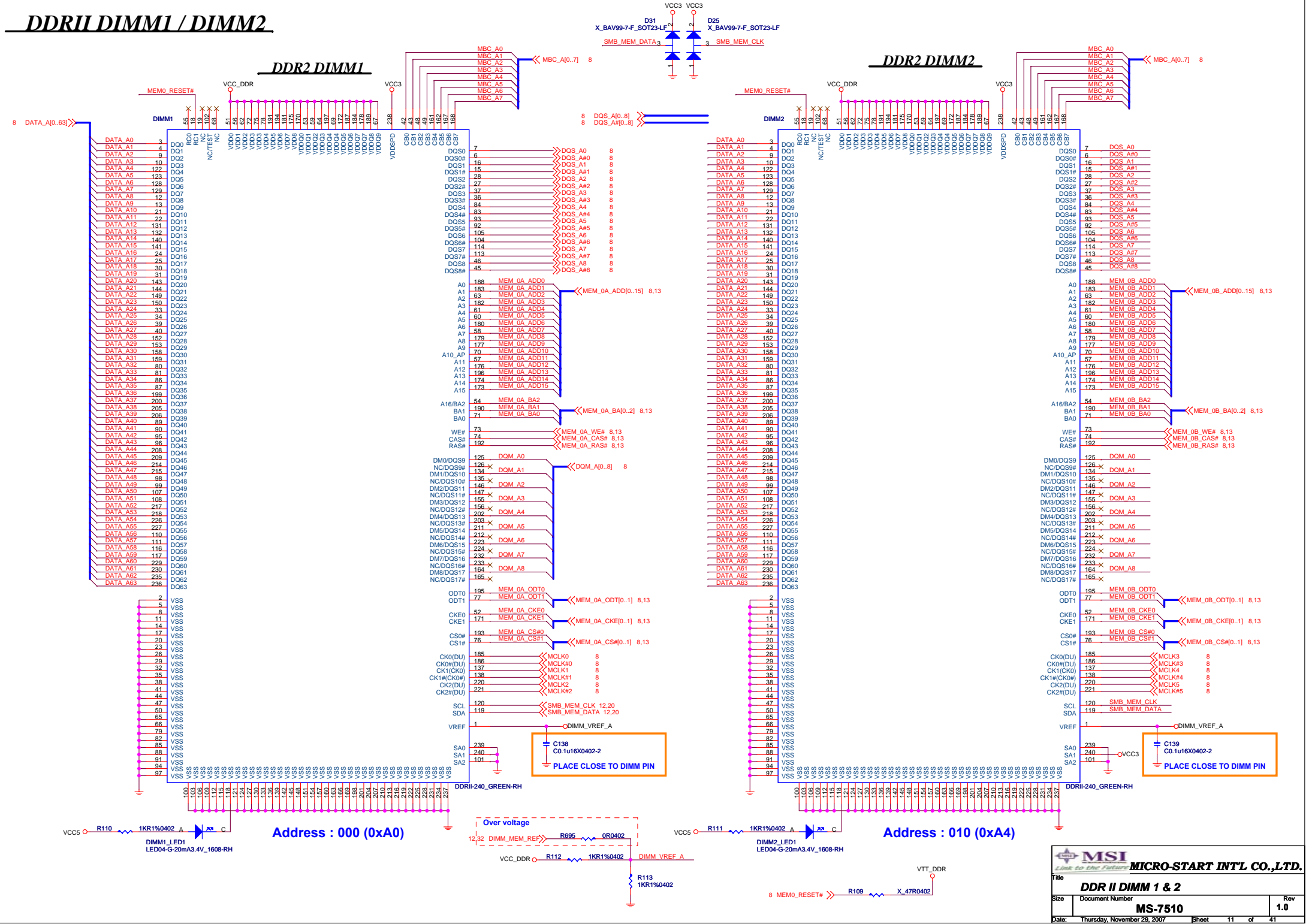
DIMM3 1A



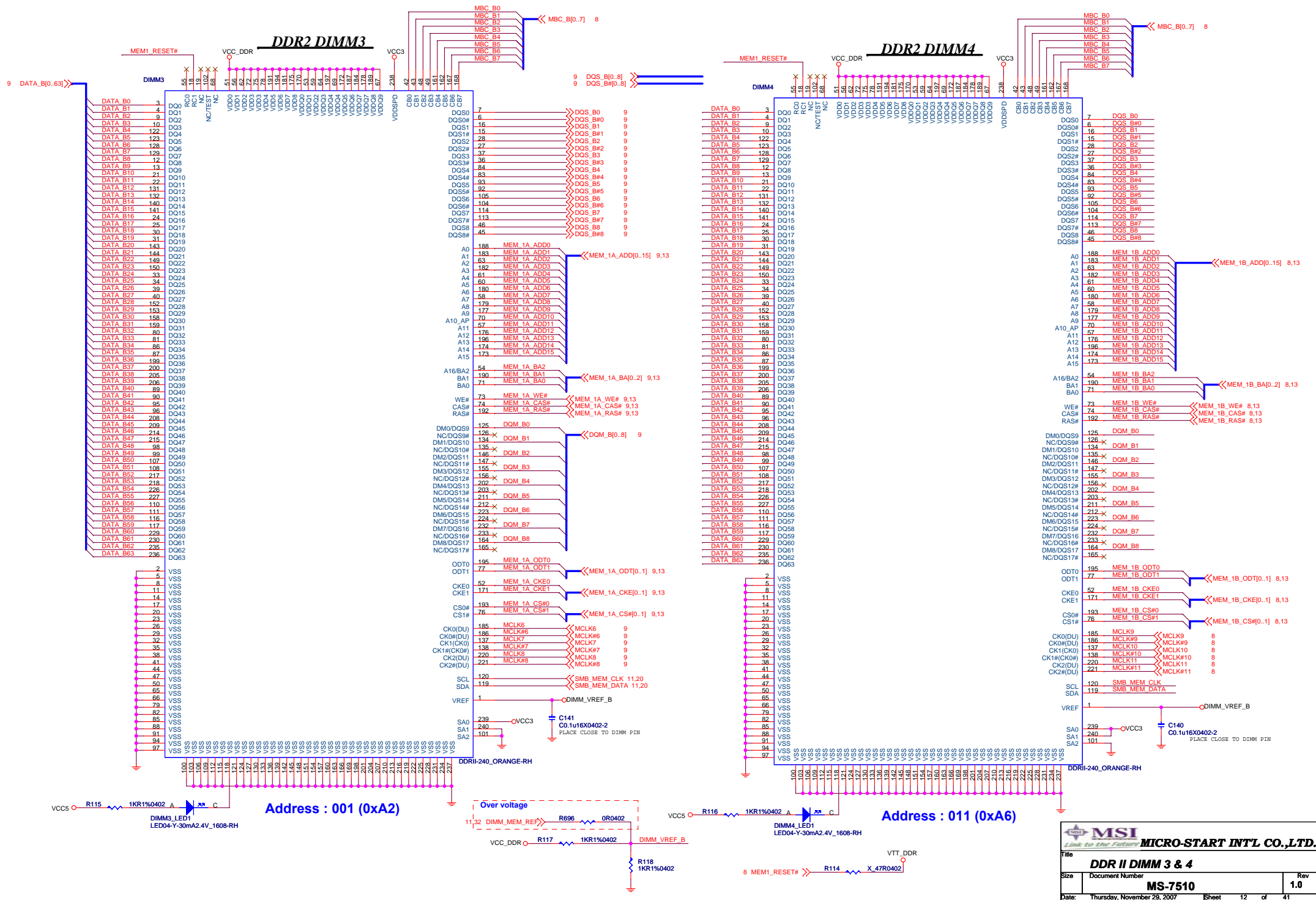
C55 - Gnd



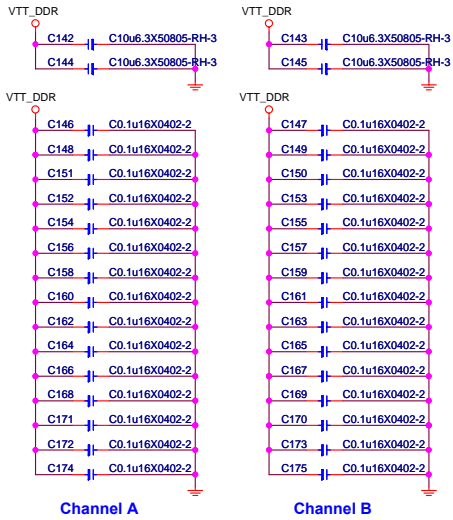
DDR1 DIMM1 / DIMM2



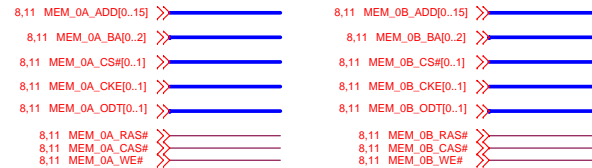
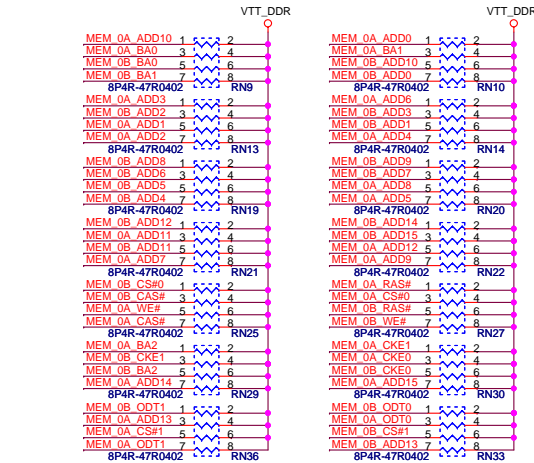
DDR1/DIMM3 / DIMM4



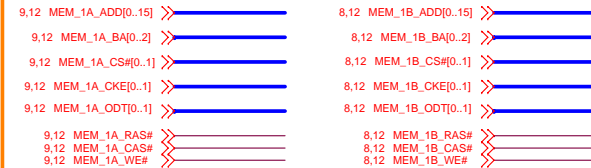
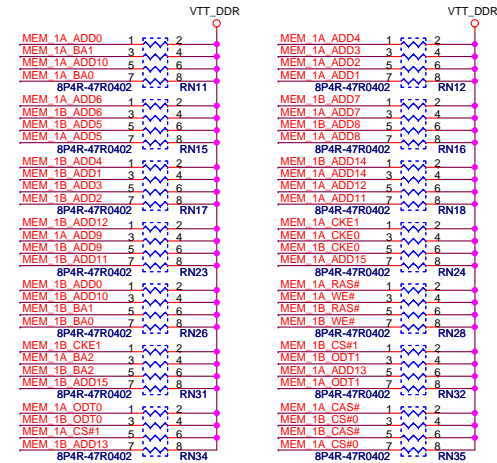
DDR Channel A VTT_DDR Decoupling Caps.



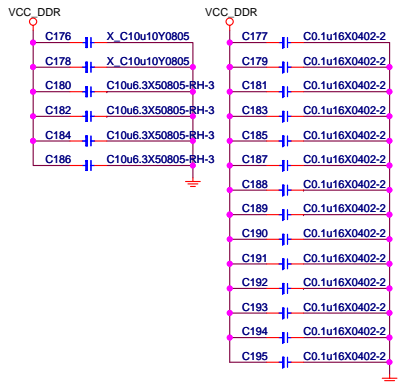
DDR Channel A Termination



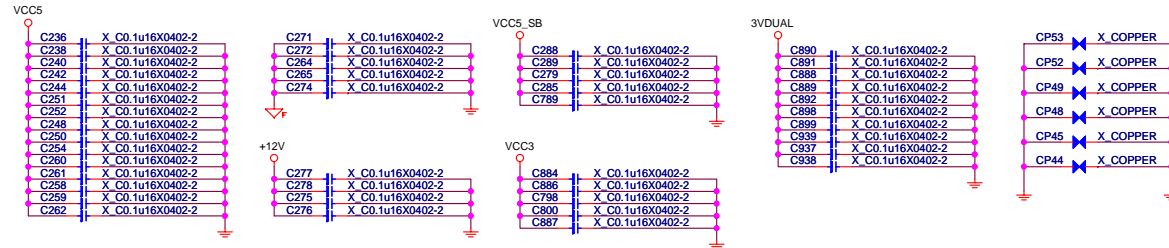
DDR Channel B Termination



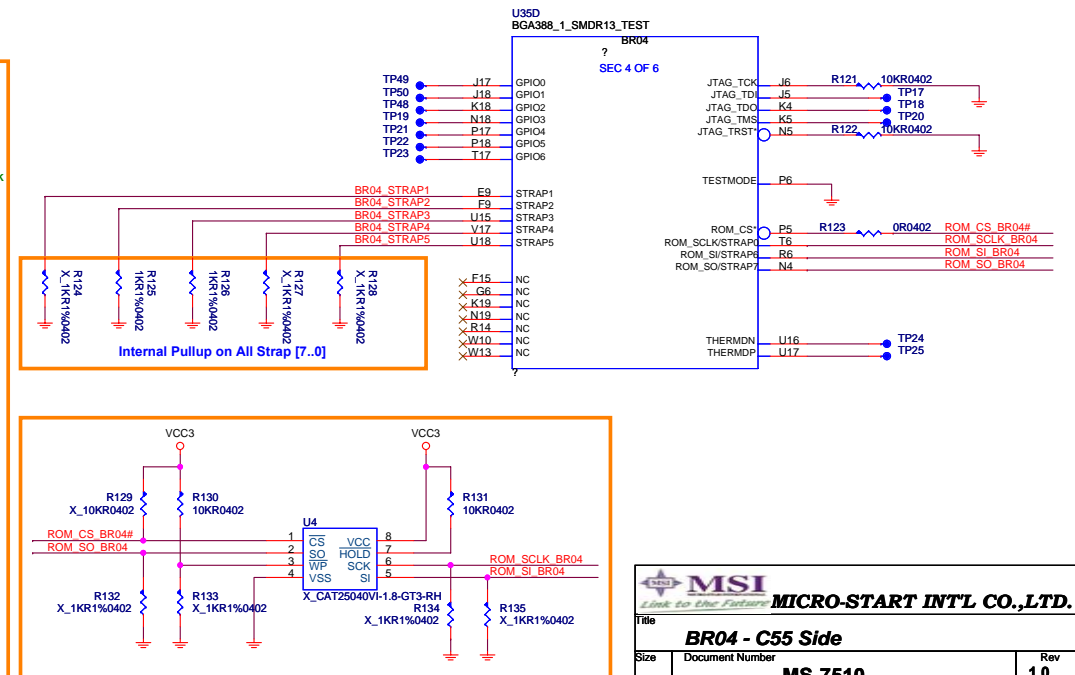
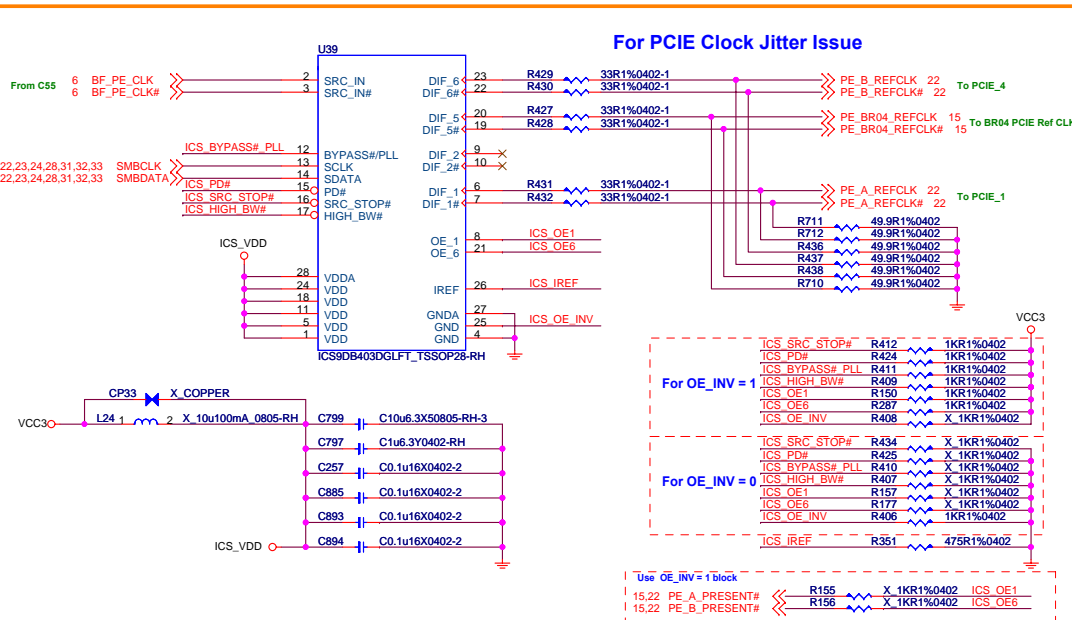
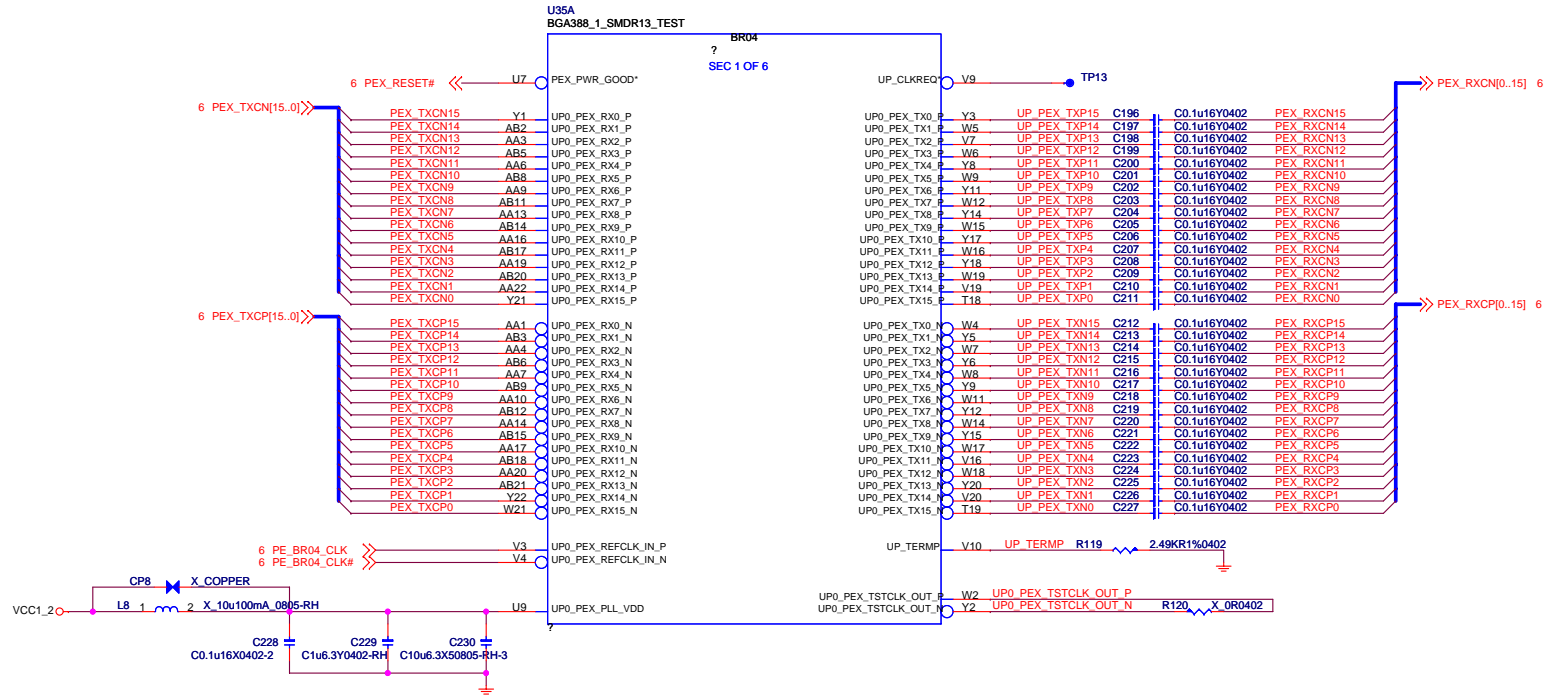
DDR Channel A VCC_DDR Decoupling Caps.



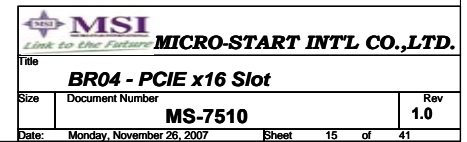
EMI Solution 2007-10-25



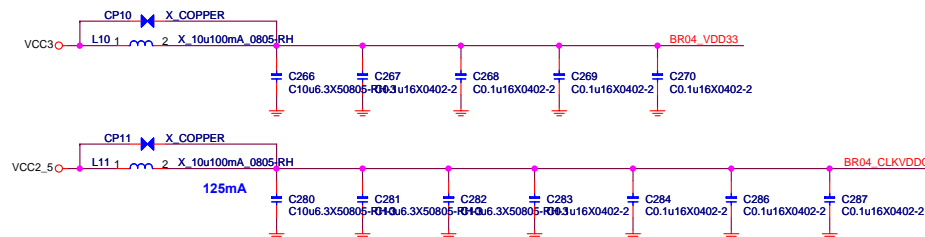
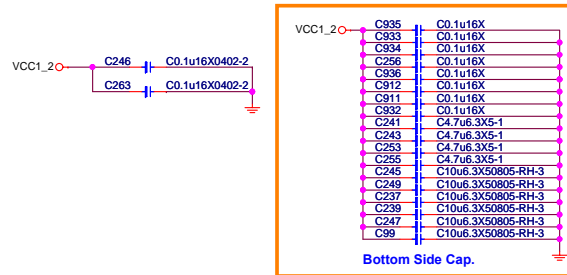
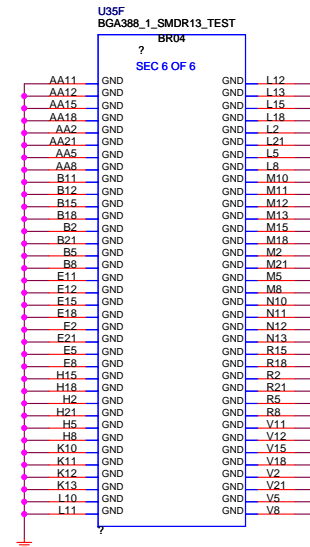
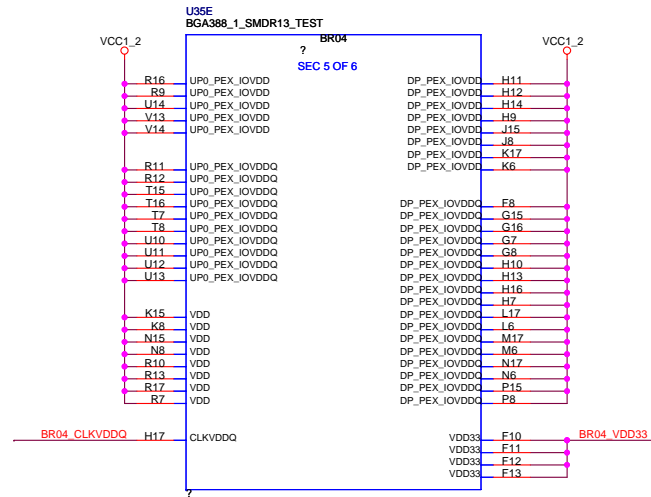
C55 to BR04 PCI-Express Interface

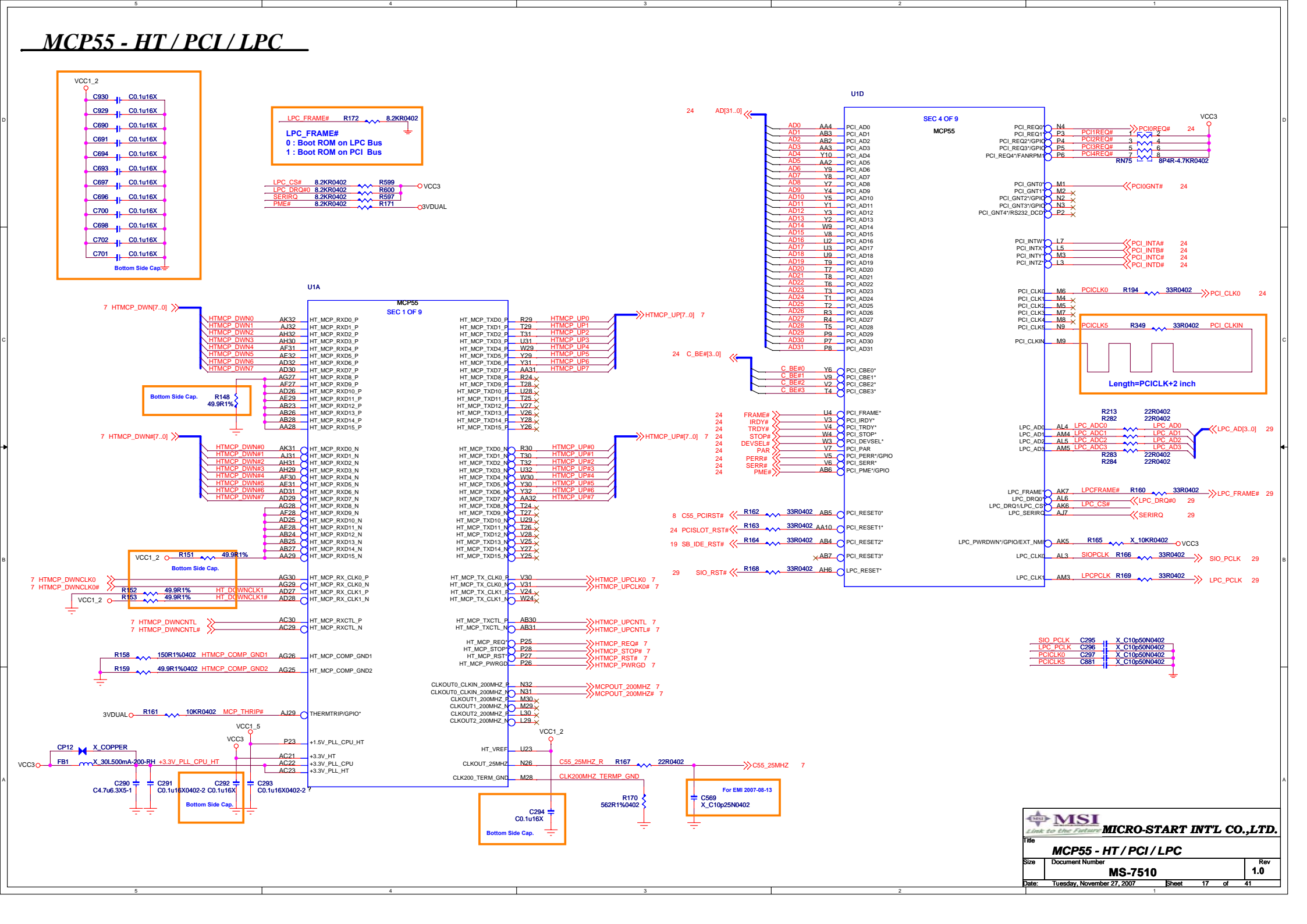


PCB layout diagram for the power plane. The diagram shows a series of decoupling capacitors (C231, C232, C233, C234, C235) connected to a common ground. A note indicates to place the capacitors close to the chipset power pin.



BR04 Power and Gnd Block



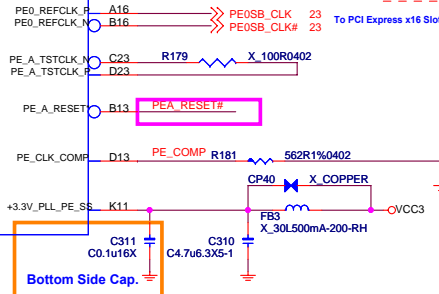
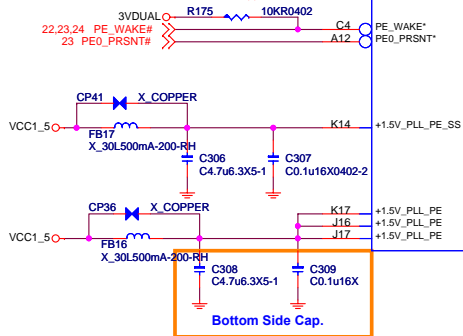
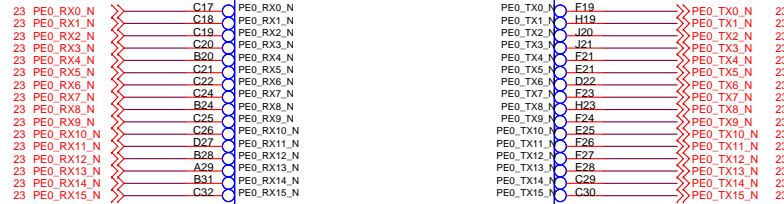
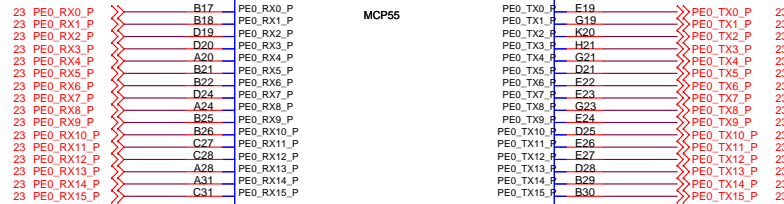


MCP55 - PCI-E

U1B

SEC 2 OF 9

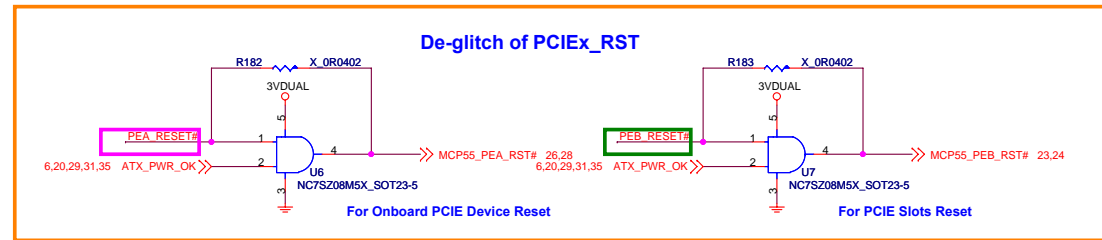
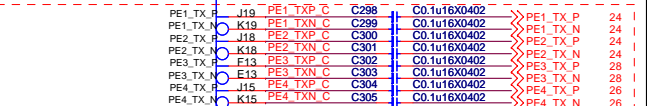
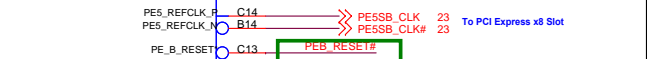
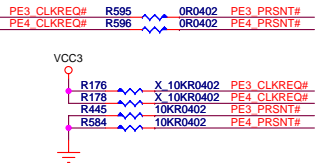
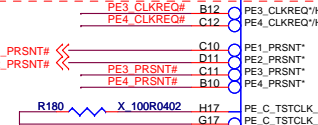
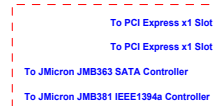
MCP55



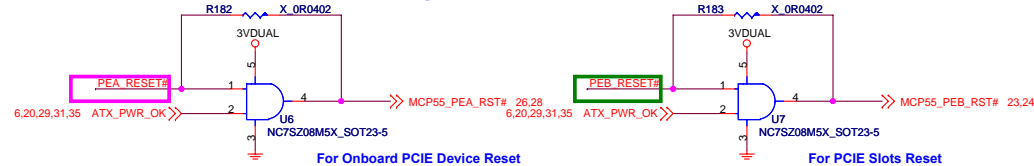
U1C

SEC 3 OF 9

MCP55

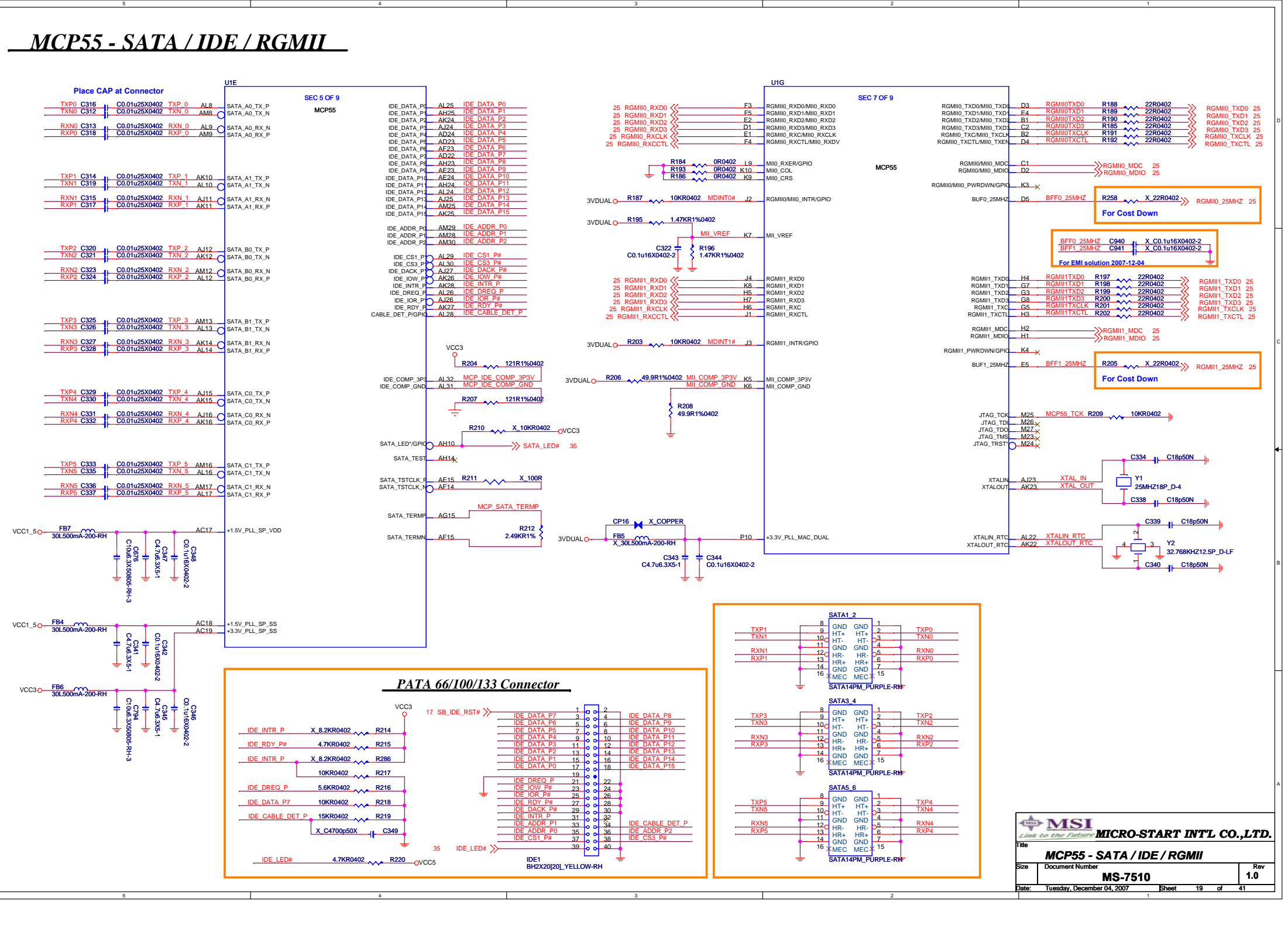
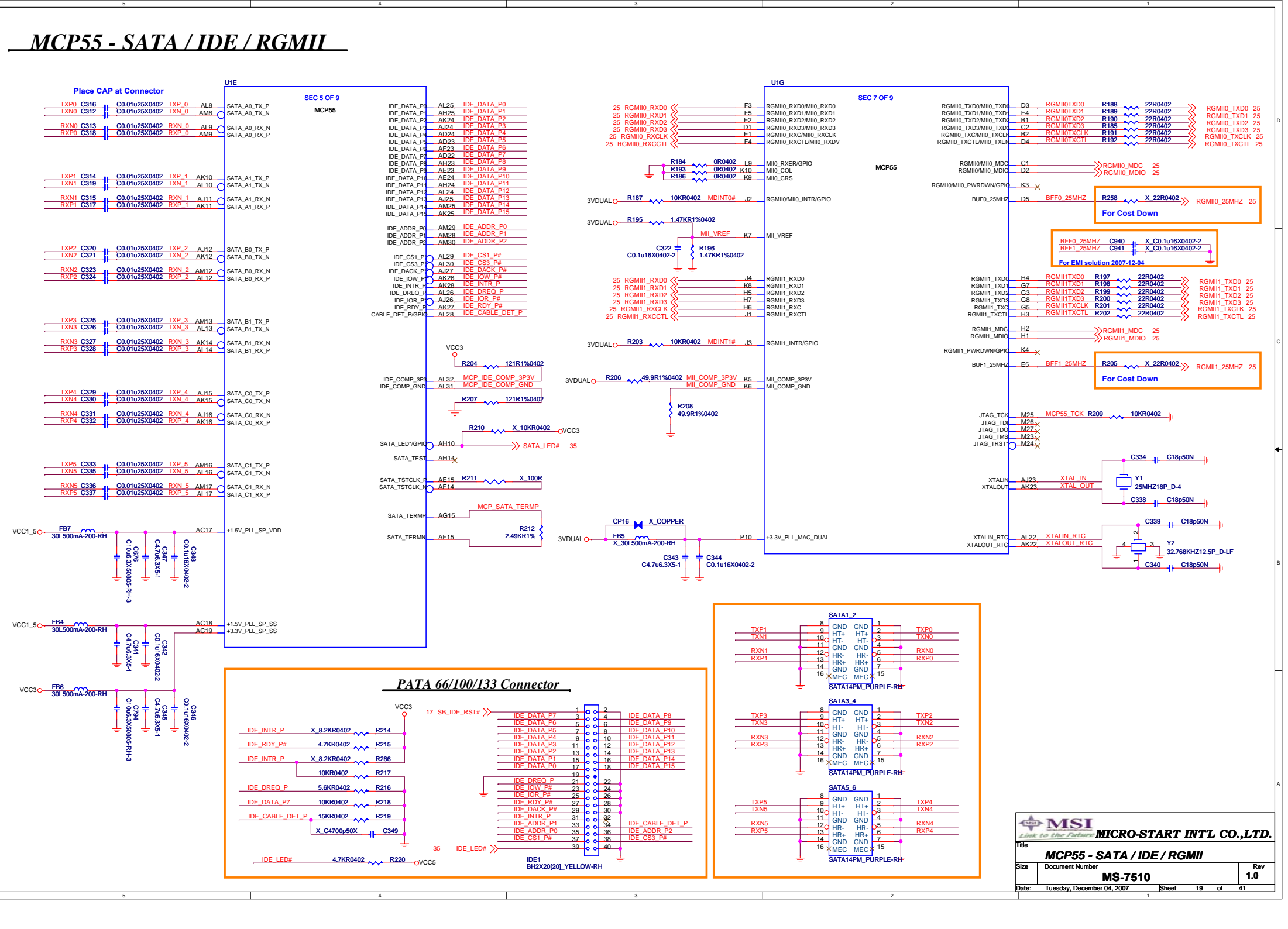


De-glitch of PCIe_RST

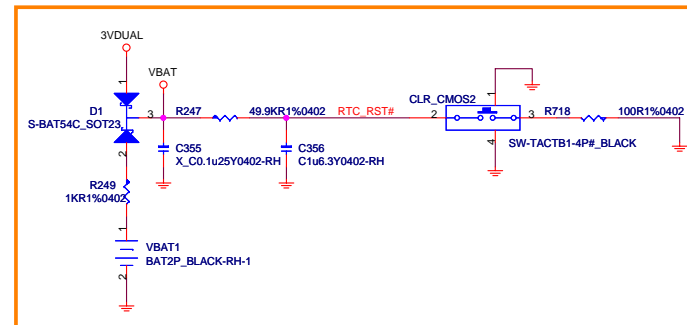
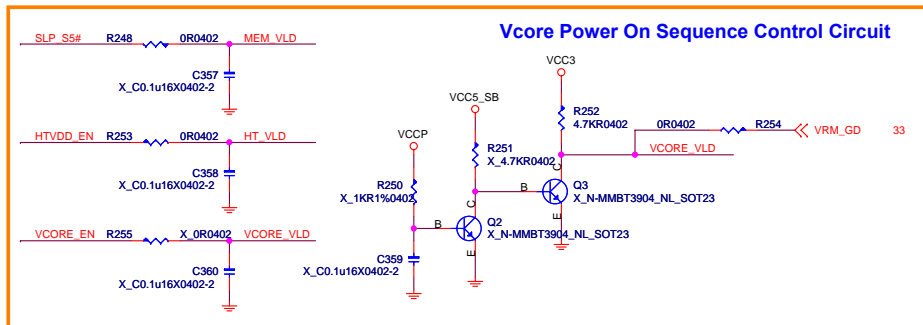
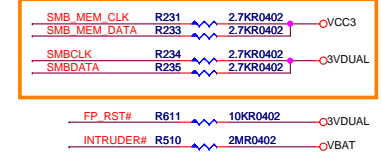
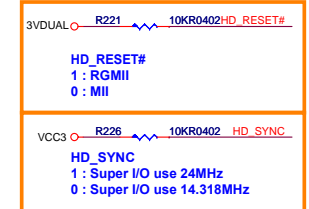
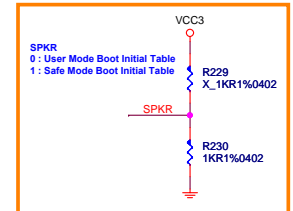
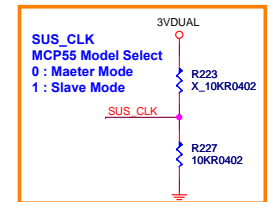
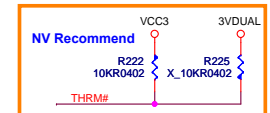
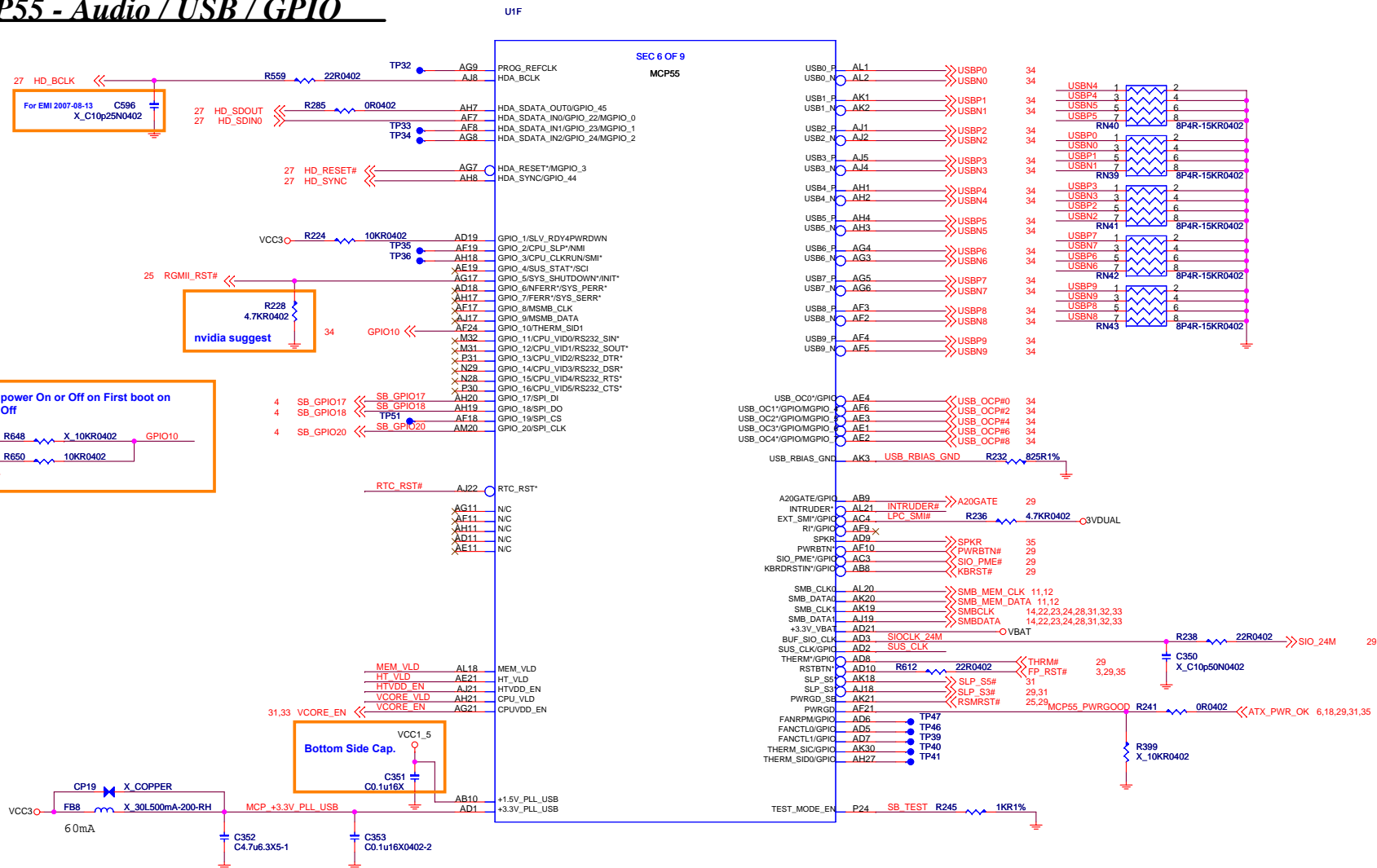


MCP55 - SATA / IDE / RGMII

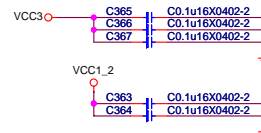
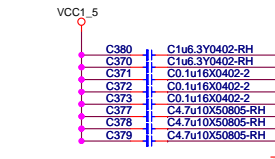
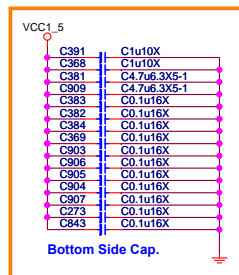
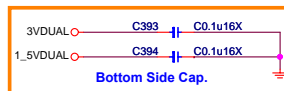
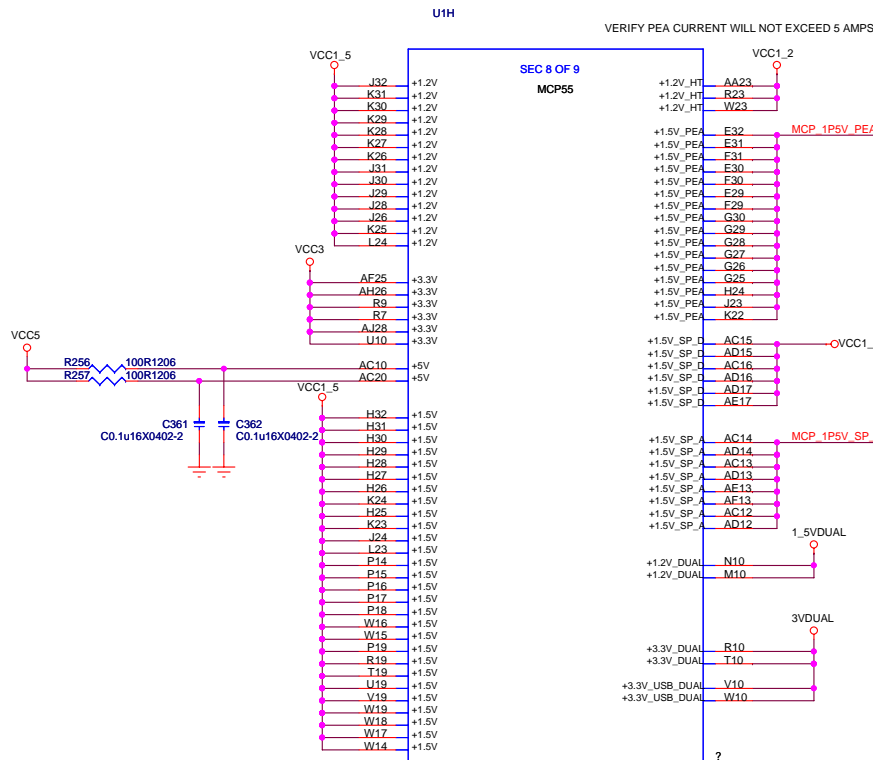
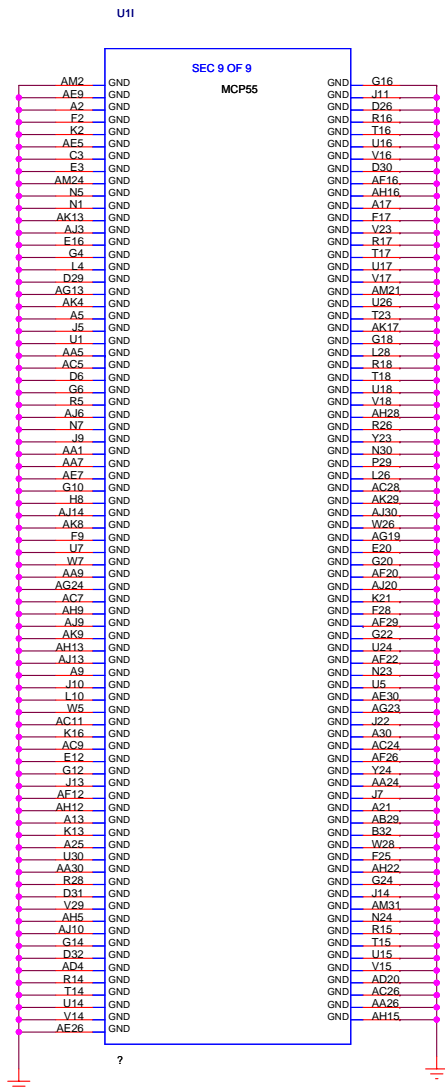
MCP55 - SATA / IDE / RGMII



MCP55 - Audio / USB / GPIO

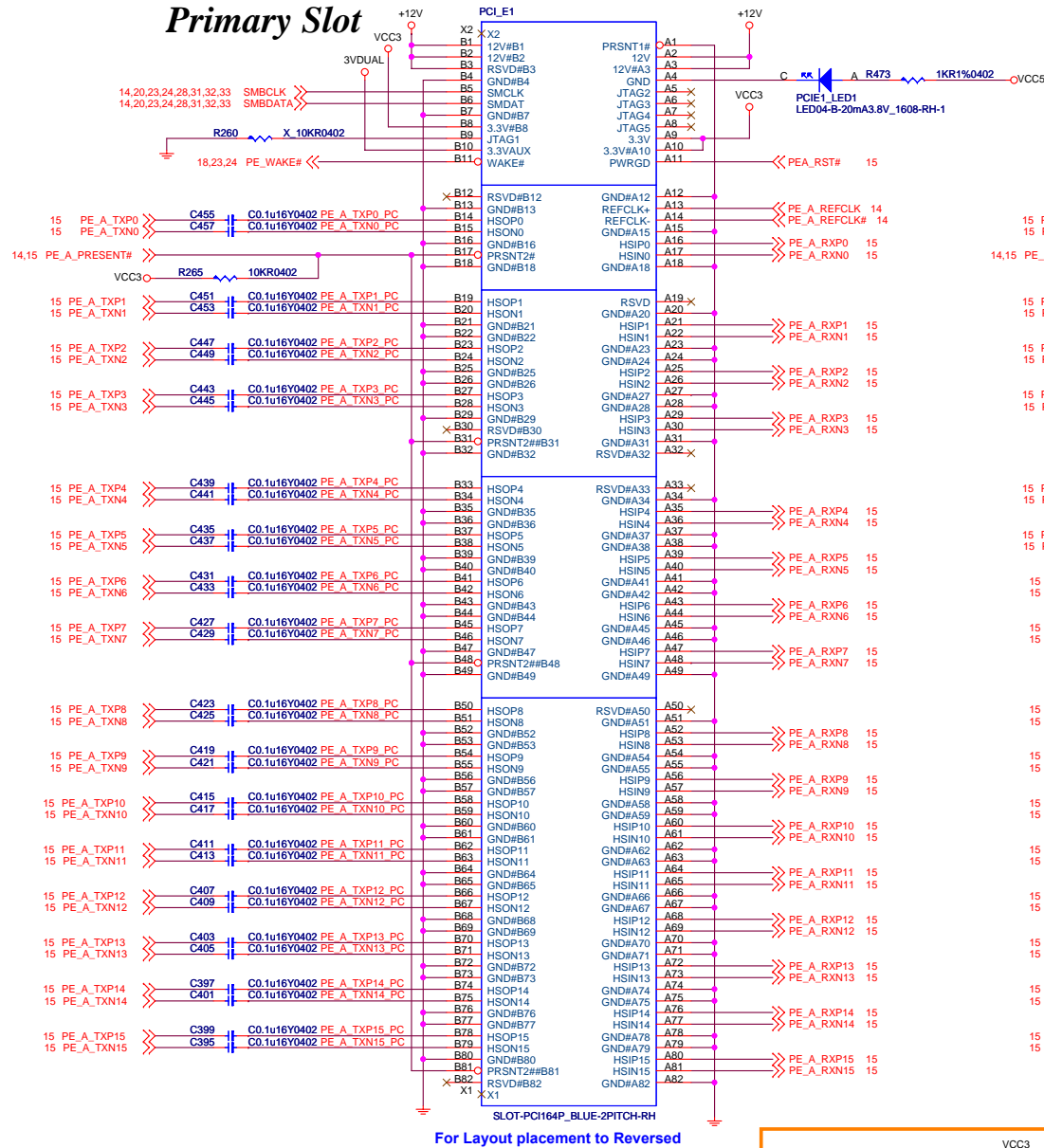


MCP55 - Power & Gnd

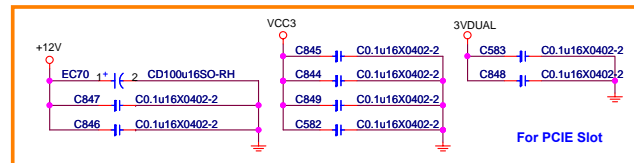
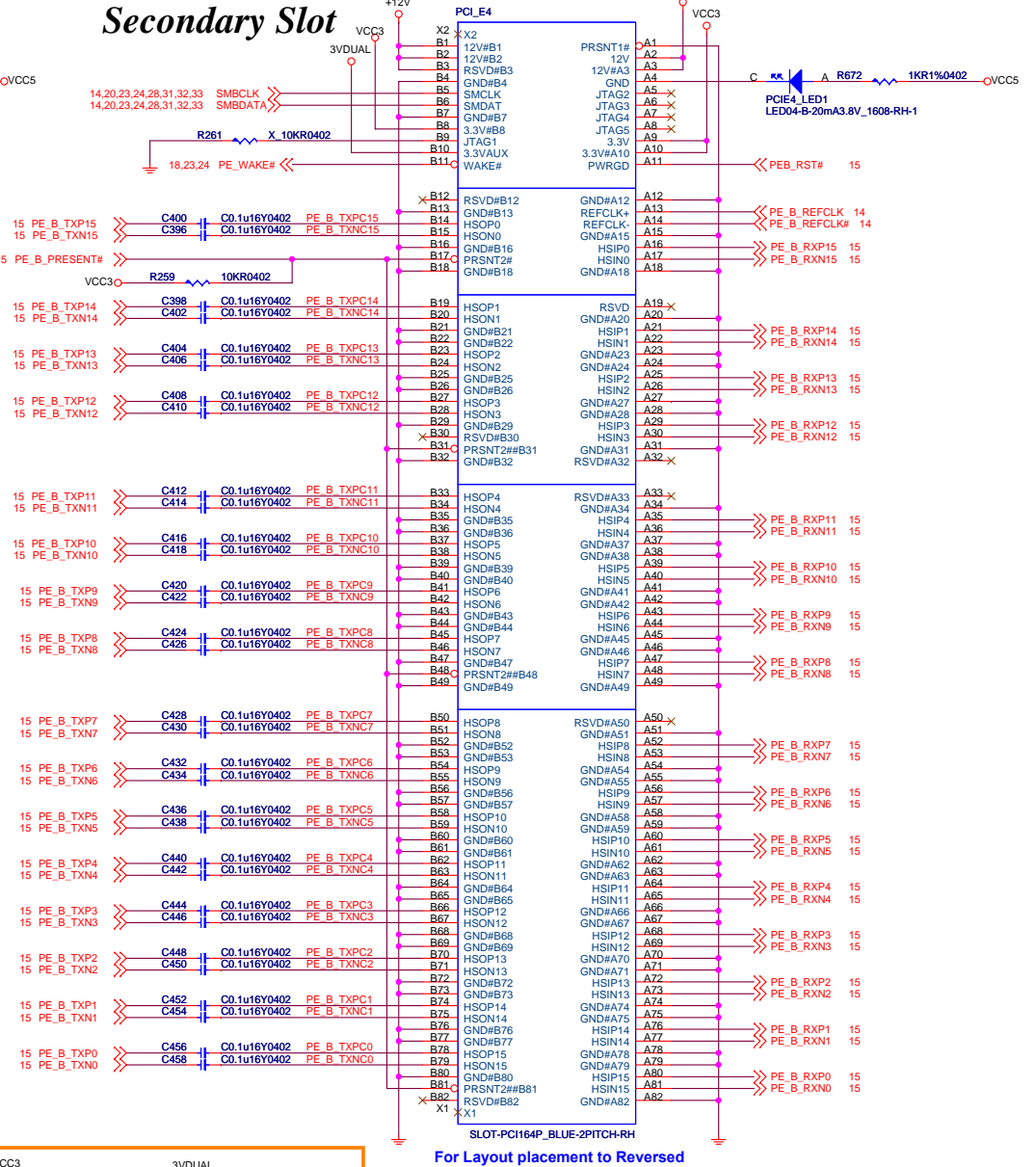


PCI-Express x16 Primary and Secondary Slot

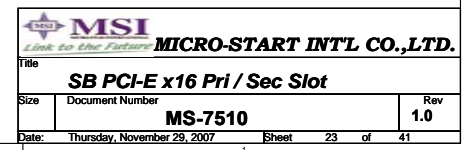
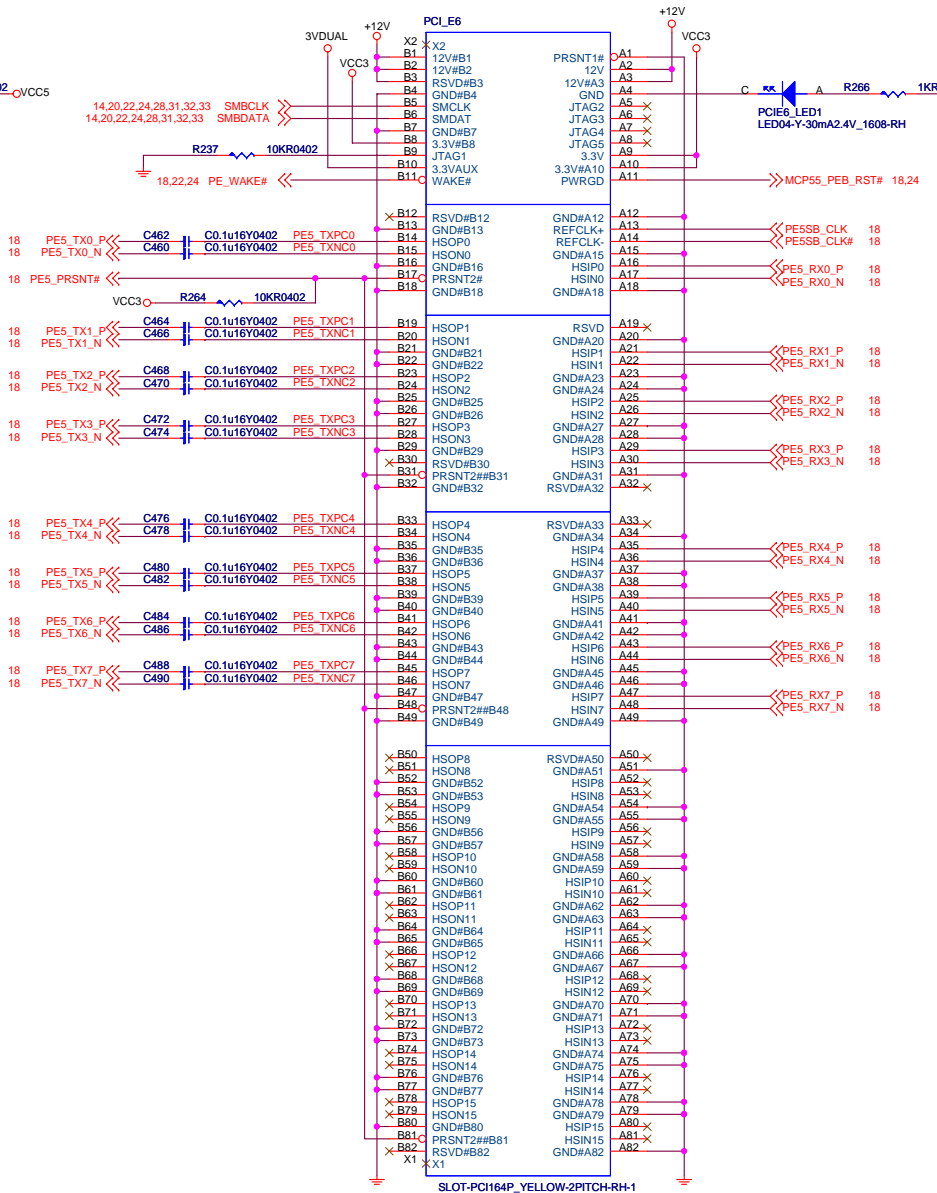
Primary Slot



Secondary Slot

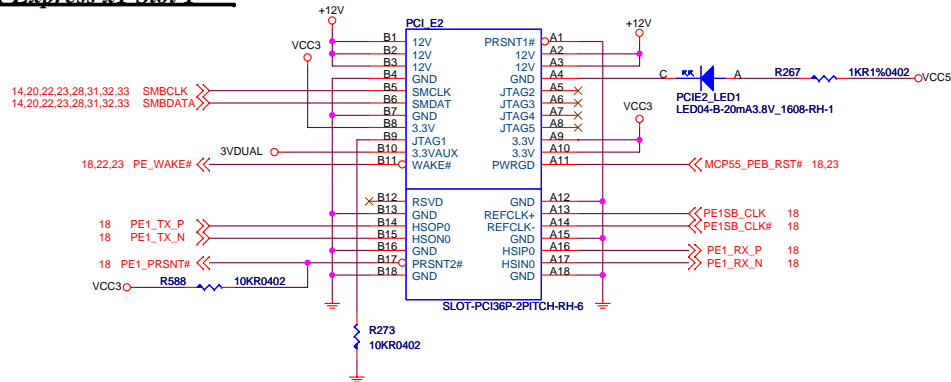


PCI Express x8 Slot

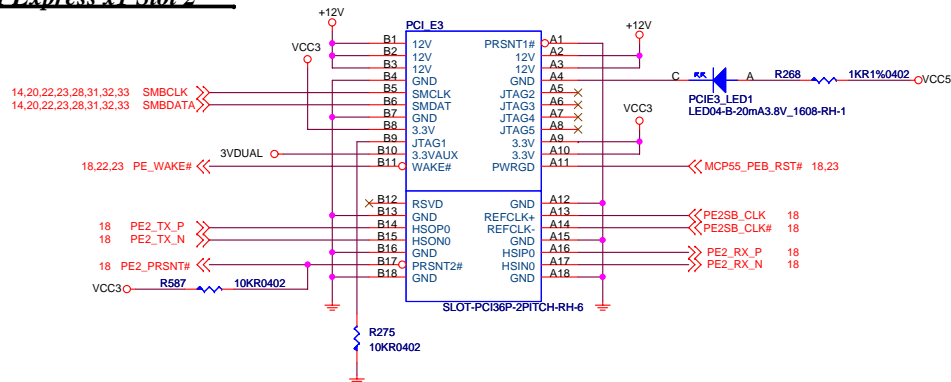


SB PCI-Express x1 Slots and PCI Slot

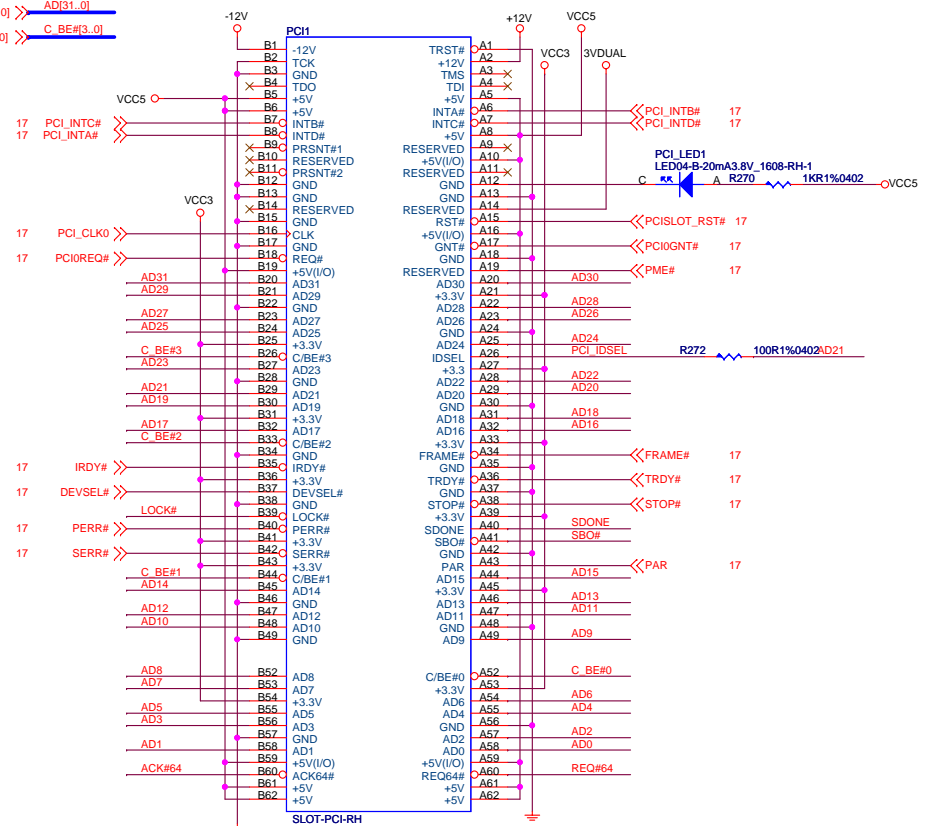
PCI Express x1 Slot 1



PCI Express x1 Slot 2

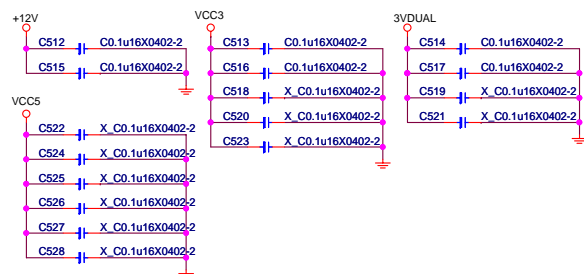


PCI Slot 1 (PCIVER: 2.2 Comply)

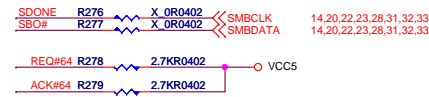
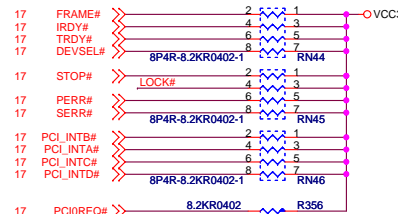


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

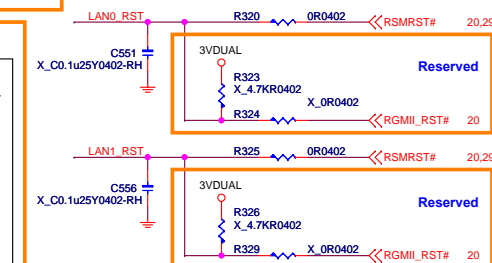
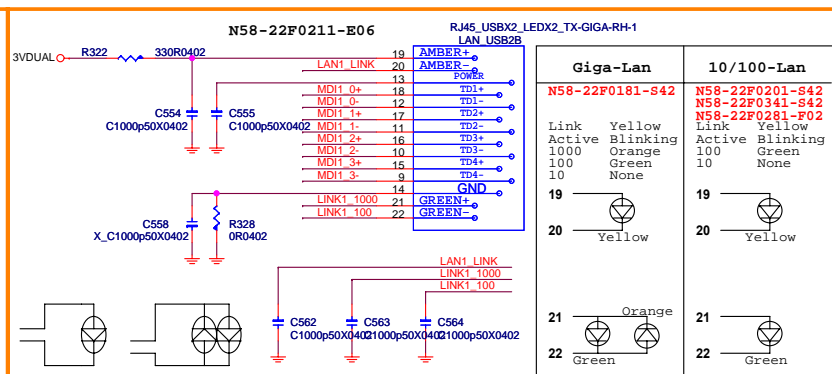
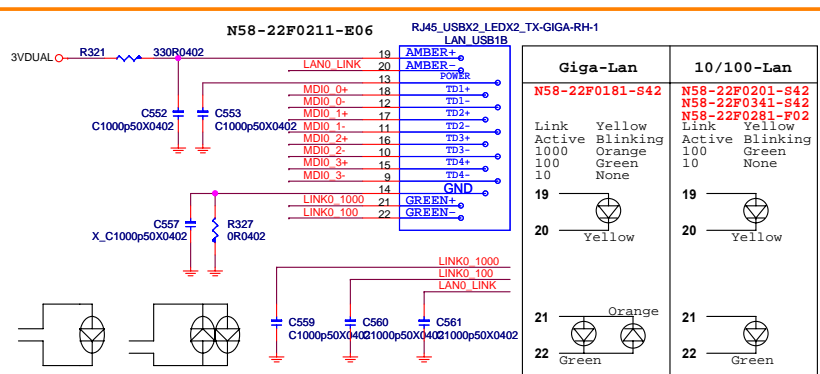
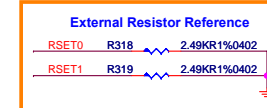
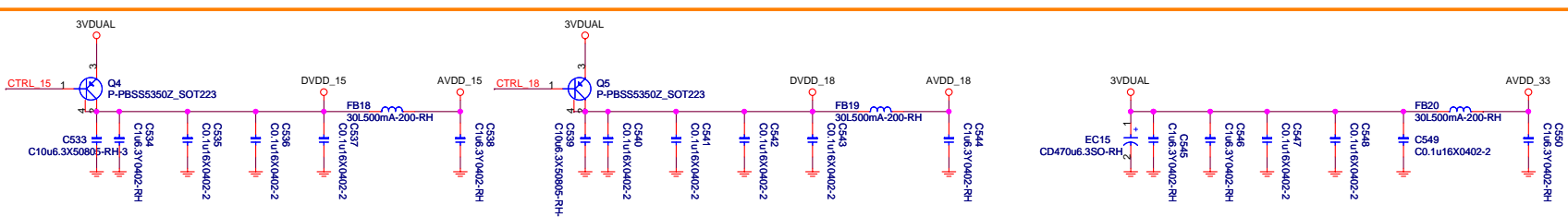
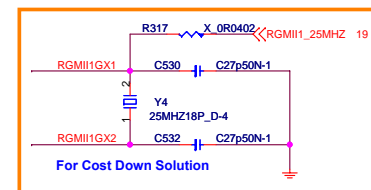
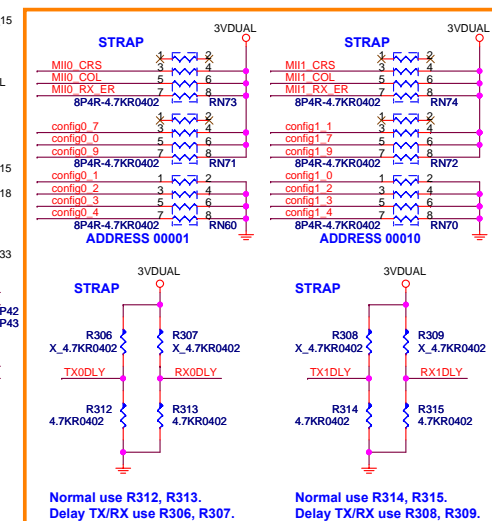
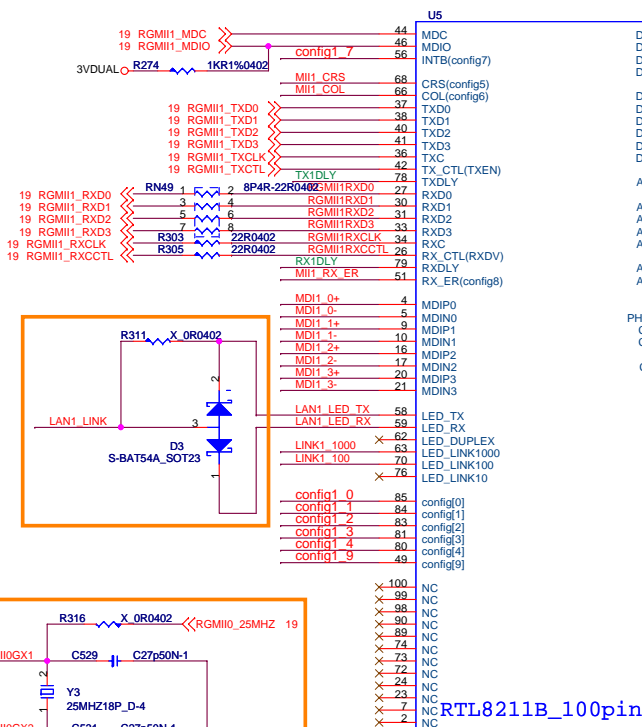
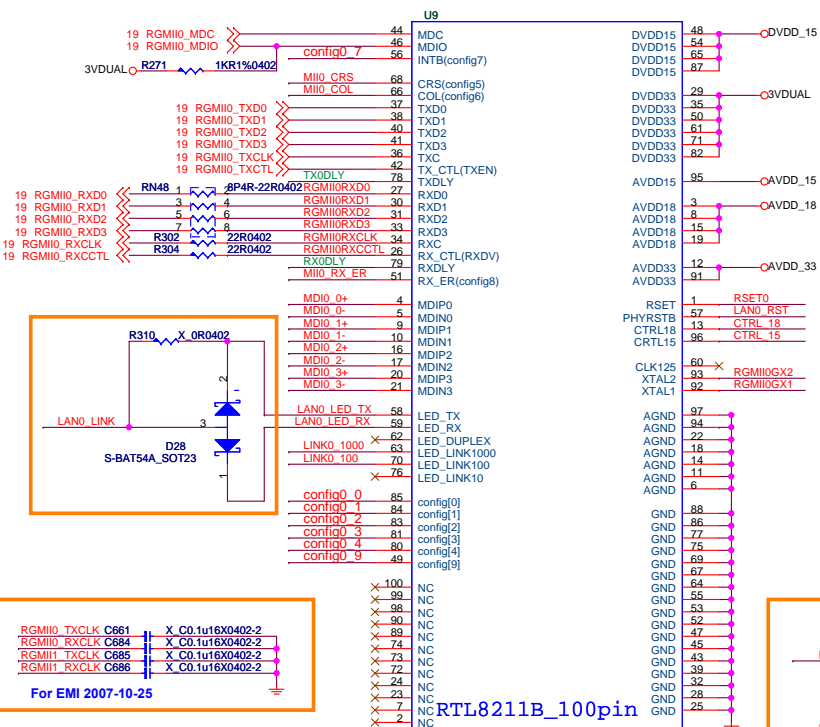
PCISlot Decoupling Capacitors



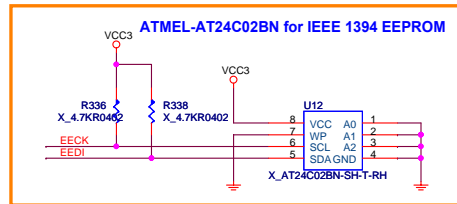
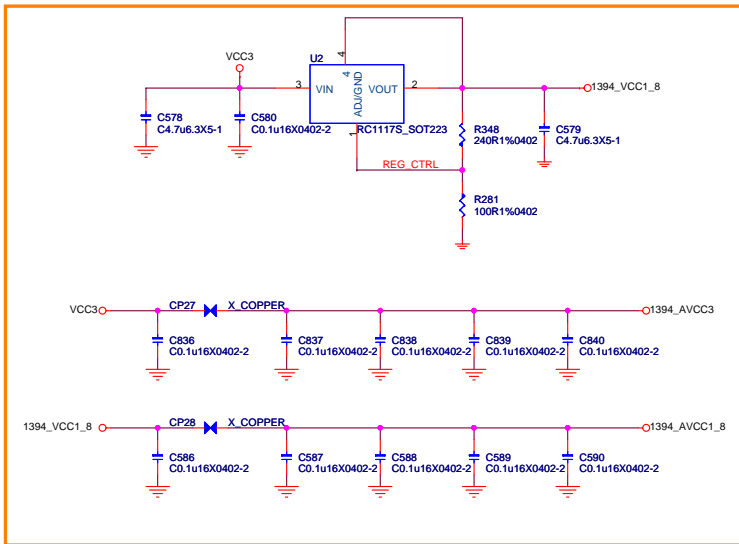
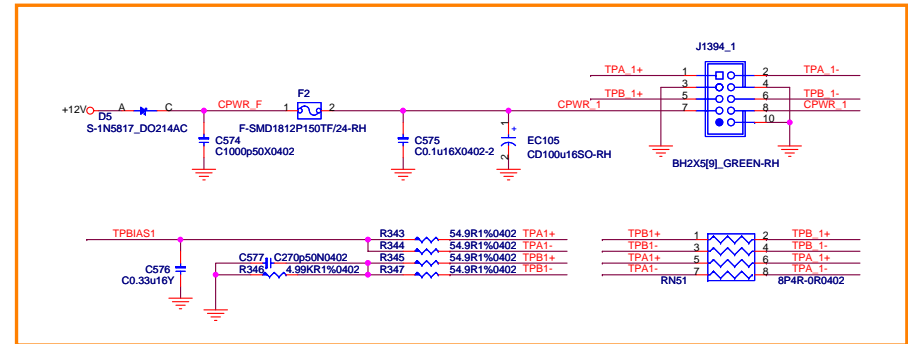
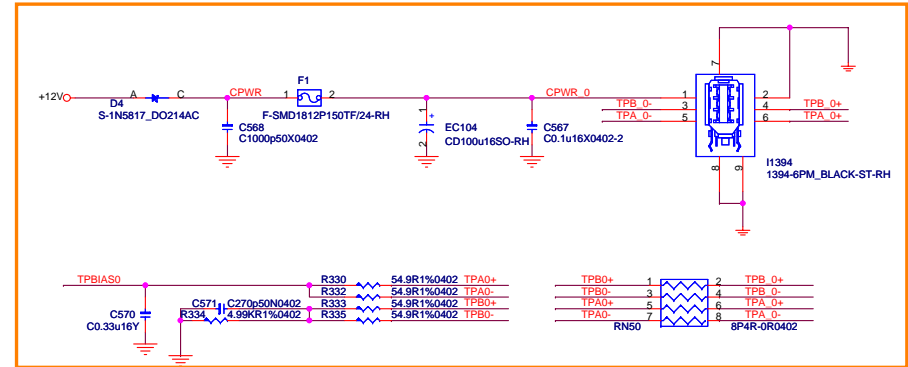
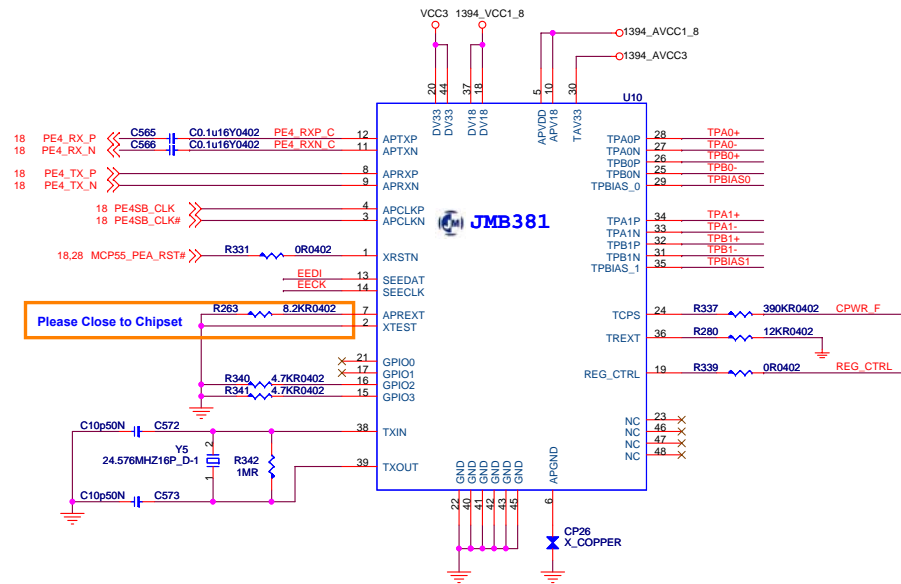
PCI Pull Up / Down Resistors



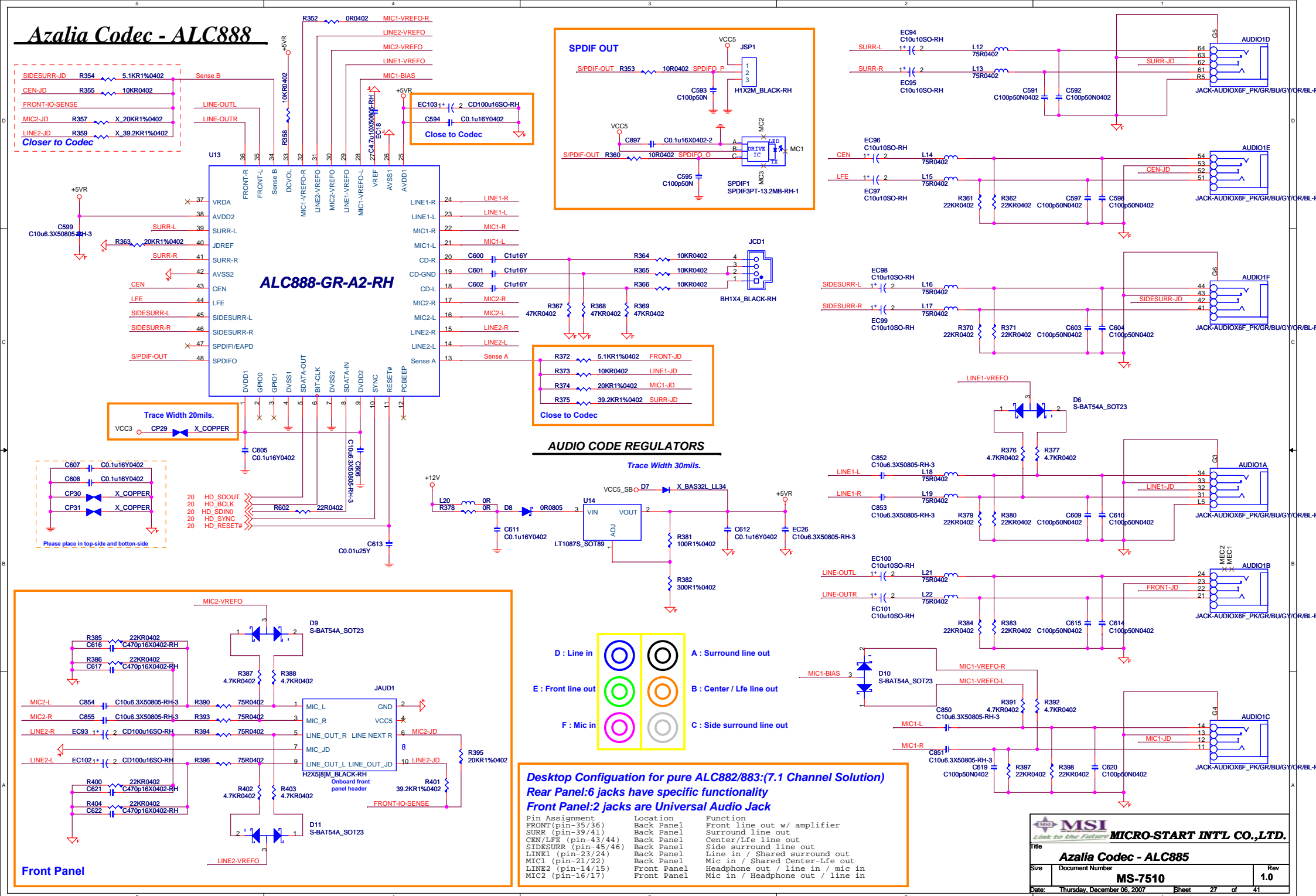
RTL8211B RGMII Gigabit PHY (Lan 1 and Lan 2)



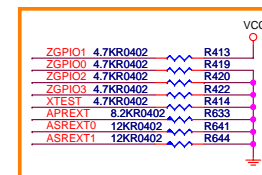
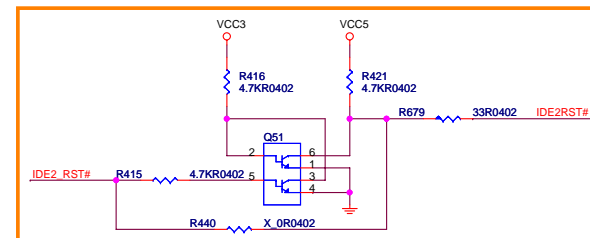
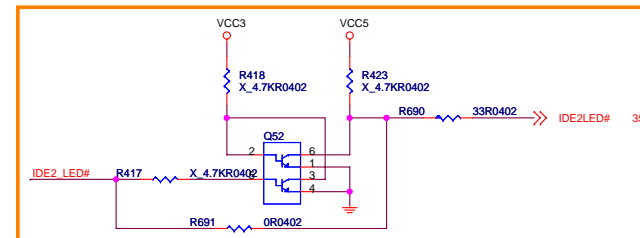
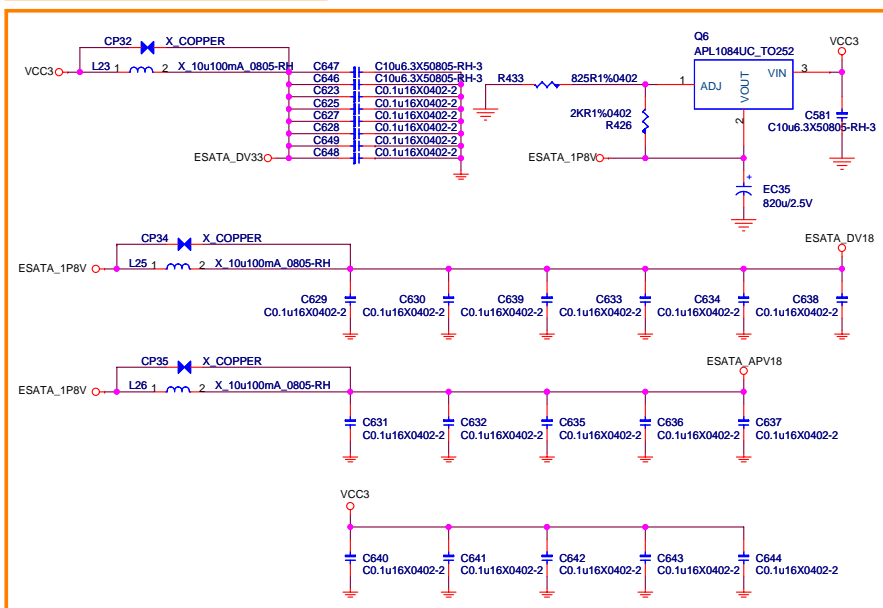
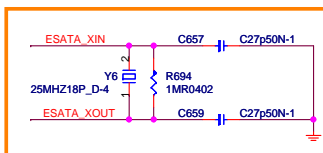
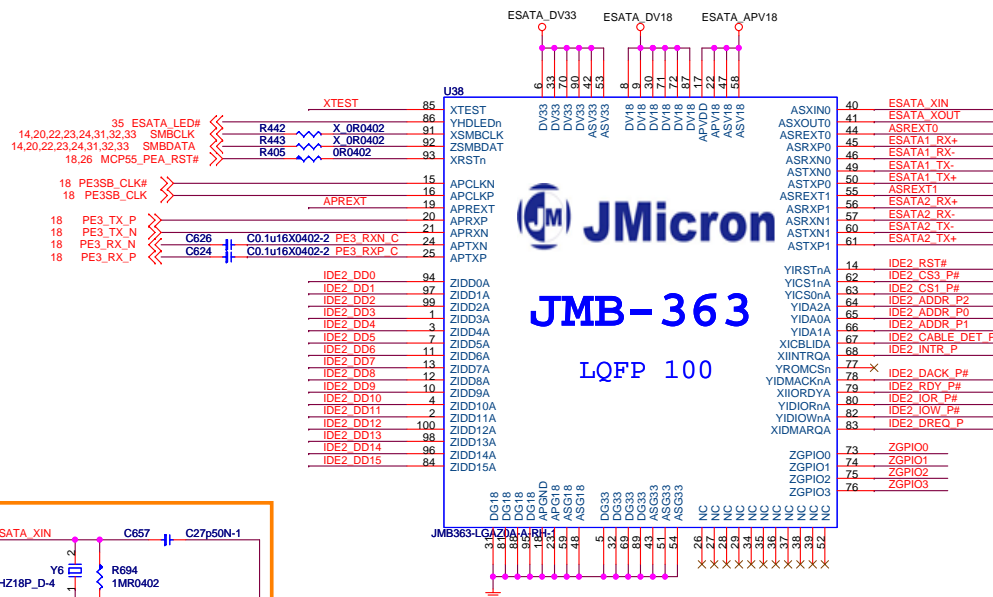
PCIE To 1394a OHCI Host Controller - JMB381



Azalia Codec - ALC888



JMicron JMB363 eSATA Controller

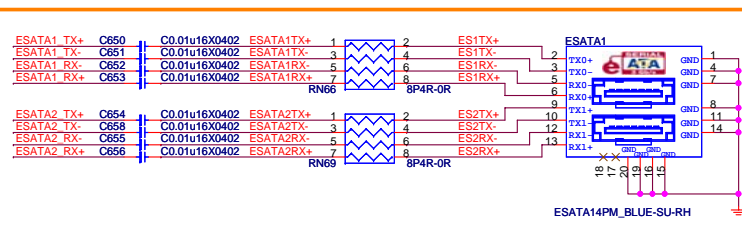
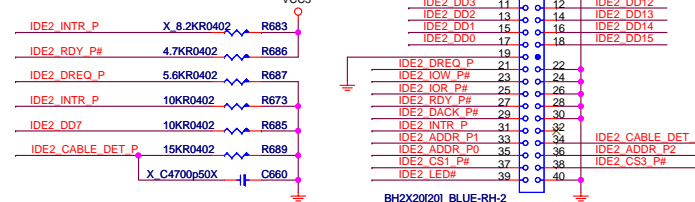


SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#48)

SATA II Port 0 External Reference Resistor.
An external 12KΩ±1%resistor should be connected and bypass to the ground ASG18 (pin#59)

PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).

PATA 66/100/133 Connector



JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function

JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0

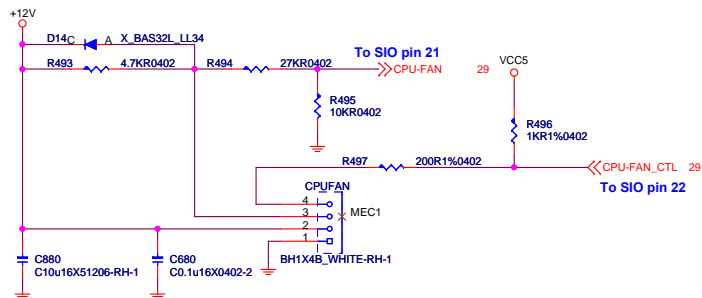
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.

JMB363 GPIO3
Reserved for debugging.

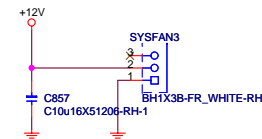
JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.

Fan Controller

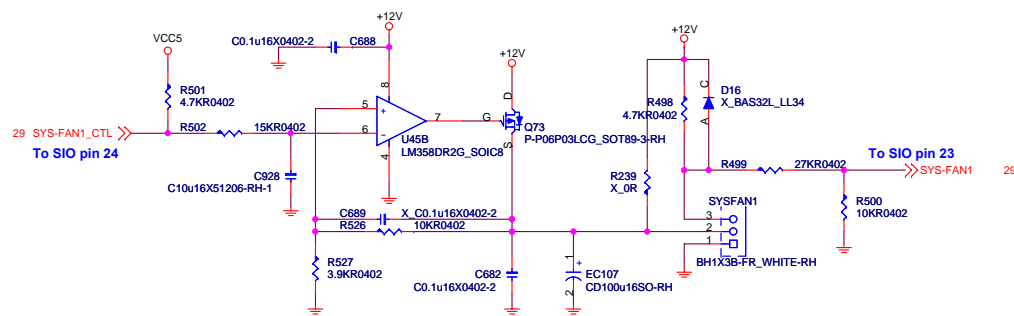
CPU Fan



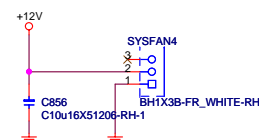
System Fan 3



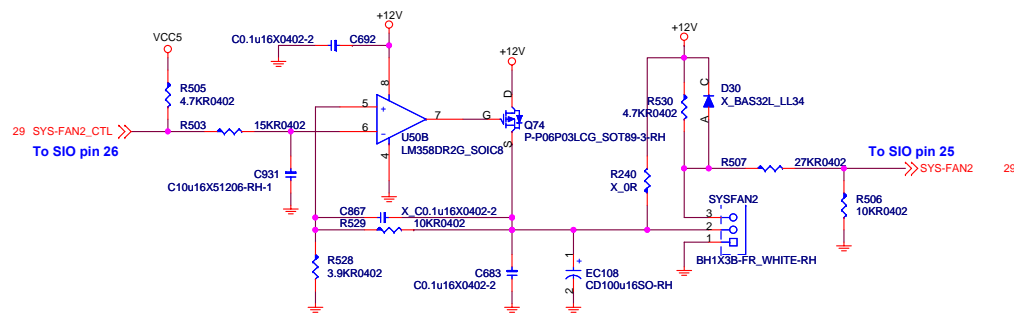
System Fan 1



System Fan 4

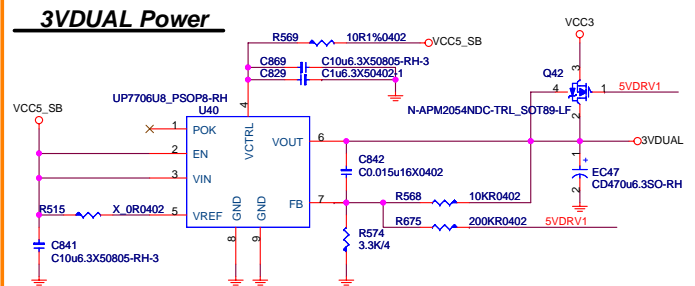


System Fan 2

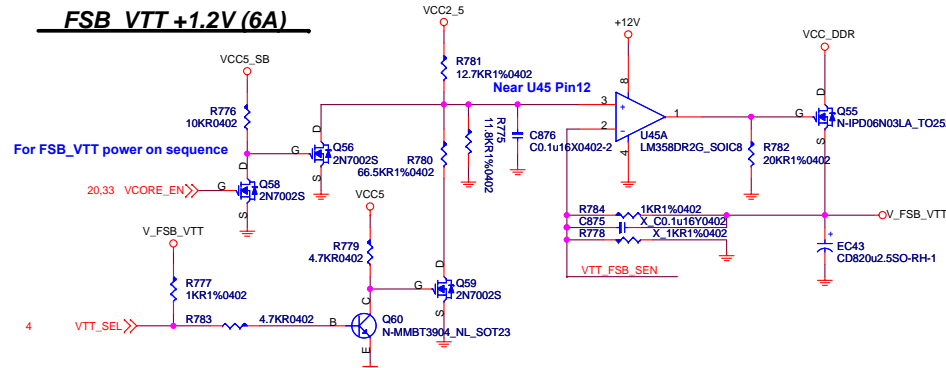


uPLACPI Solution

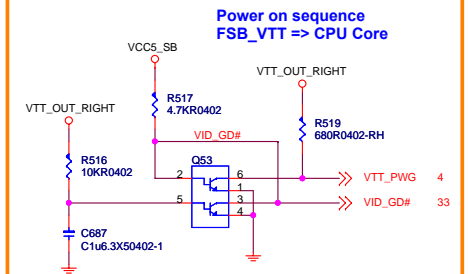
3VDUAL Power



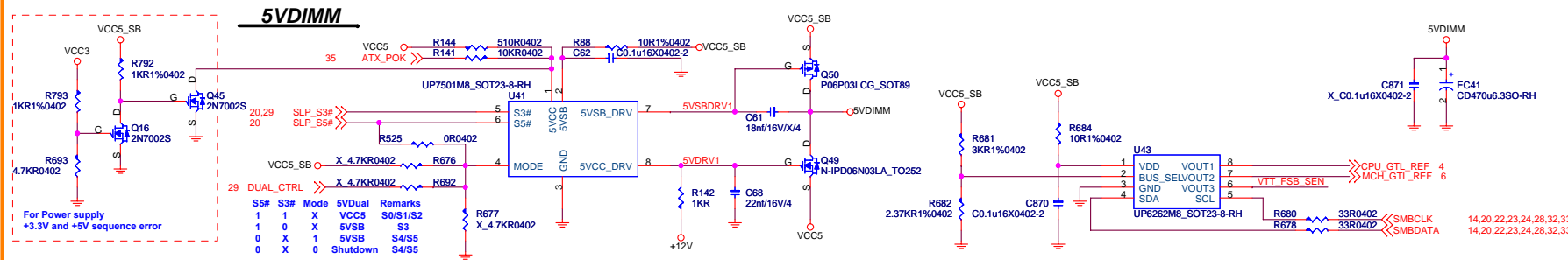
FSB VTT +1.2V (6A)



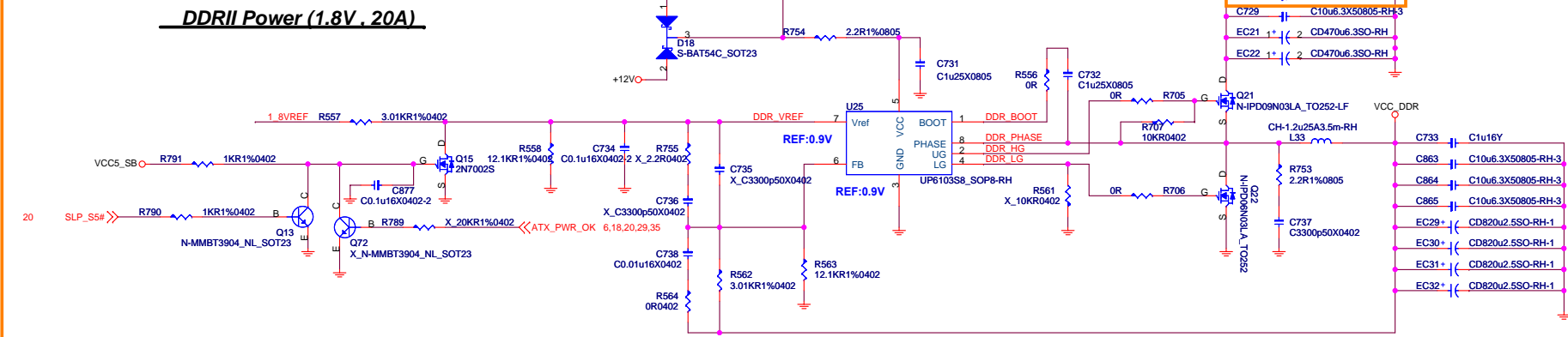
Power on sequence
FSB_VTT => CPU Core



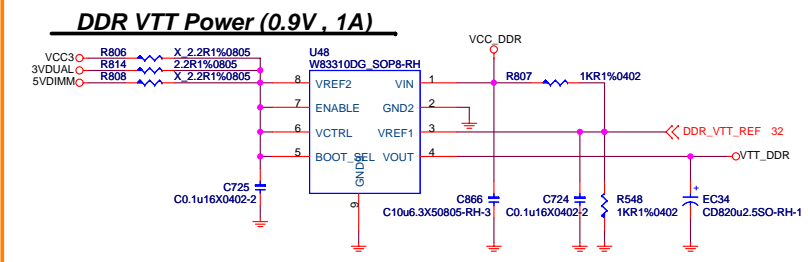
5VDIMM



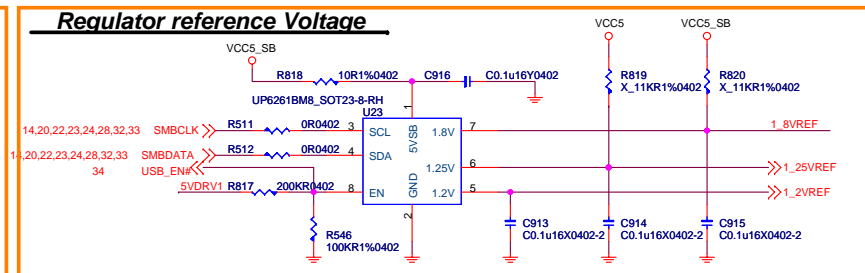
DDRII Power (1.8V, 20A)



DDR VTT Power (0.9V, 1A)



Regulator reference Voltage

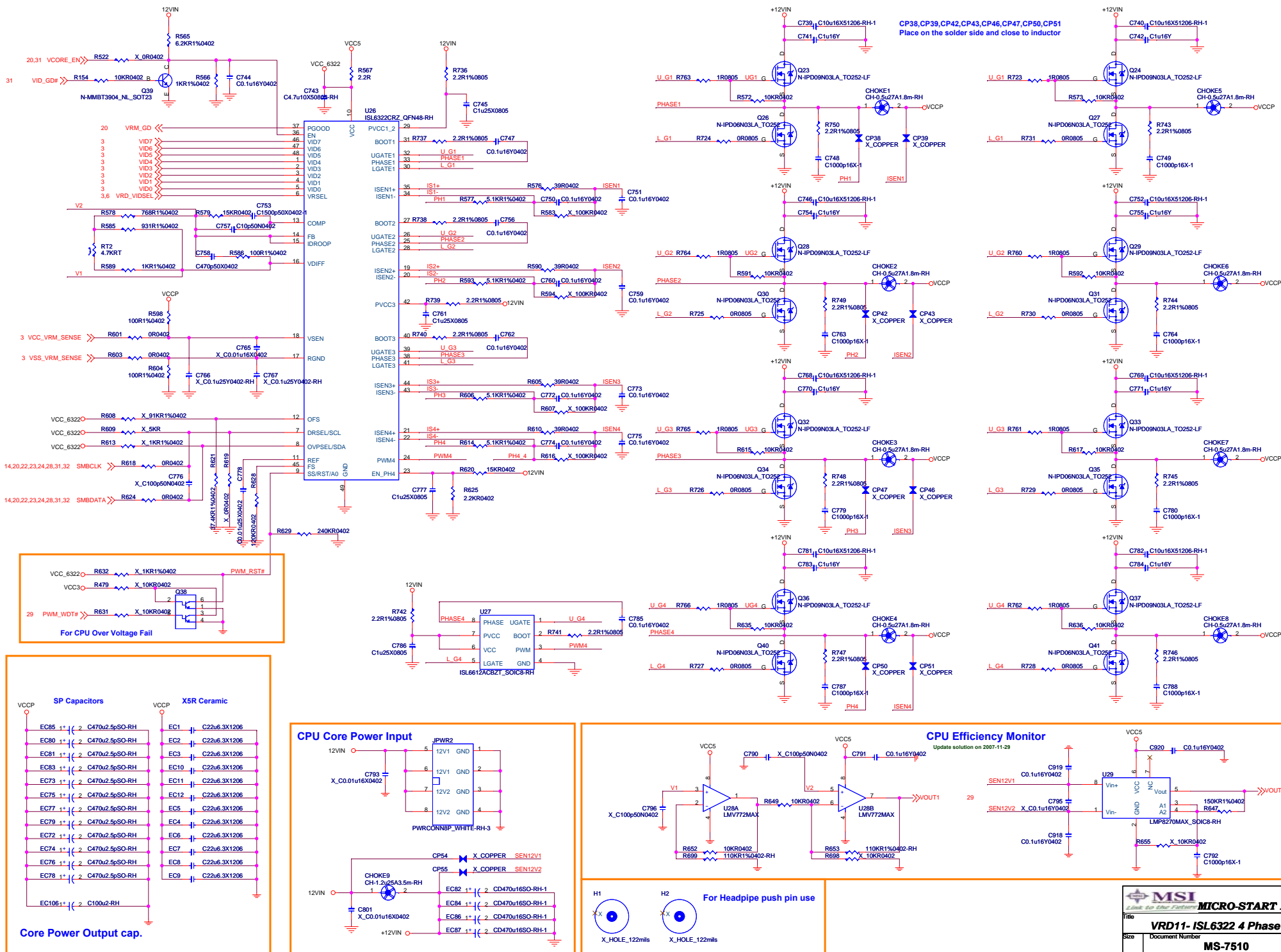


Title			
MS12 ACPI Controller			
Size	Document Number		Rev
	MS-7510		1.0
Date:	Thursday, December 06, 2007	Sheet	31 of 41

C55 + BR04 1.2V Core Power (25A + 10A)

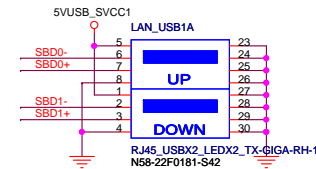
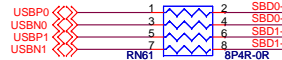
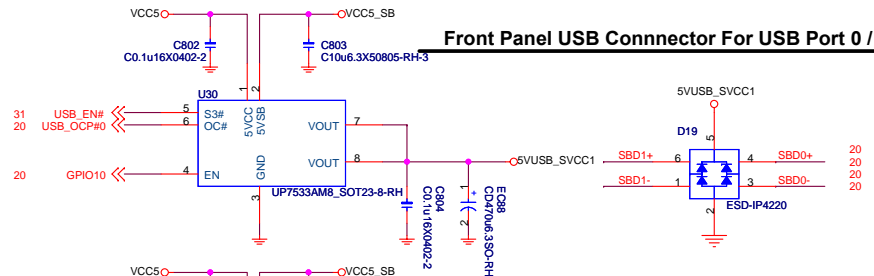


Voltage Regular Module (VRD11)

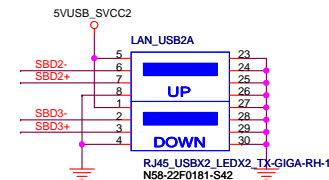
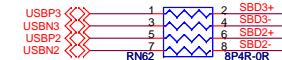
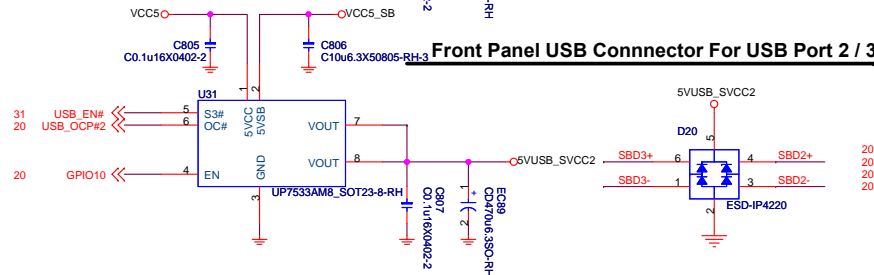


Front Panel and Real I/O USB Connector

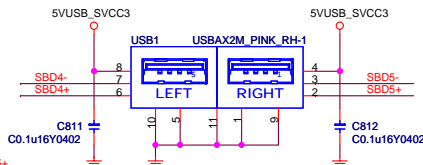
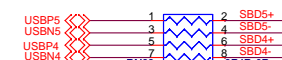
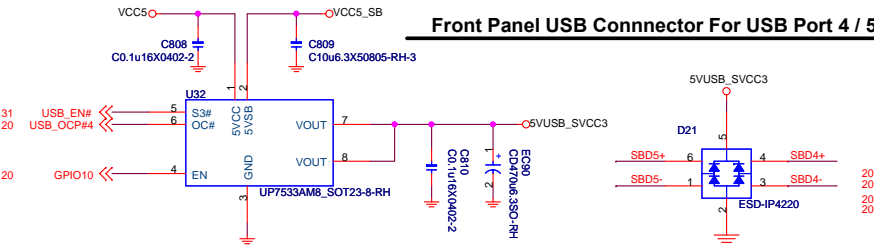
Front Panel USB Connector For USB Port 0 / 1



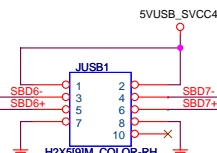
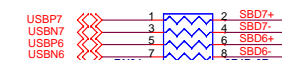
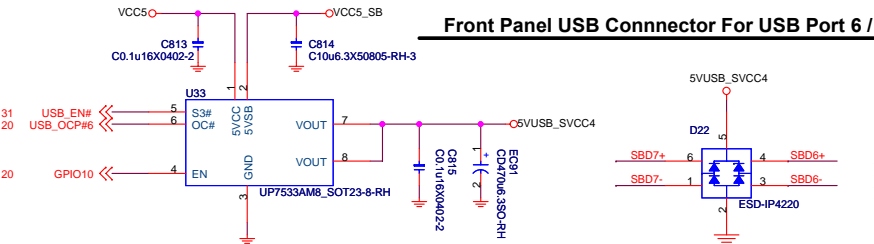
Front Panel USB Connector For USB Port 2 / 3



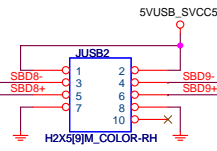
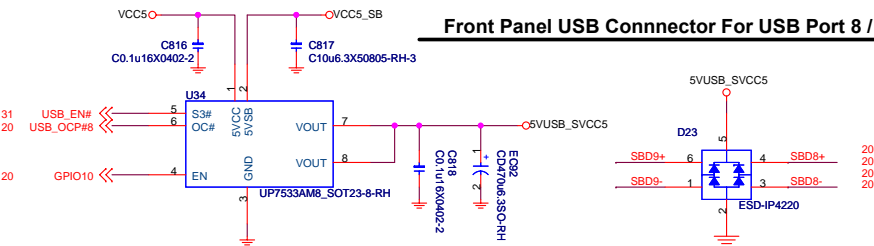
Front Panel USB Connector For USB Port 4 / 5



Front Panel USB Connector For USB Port 6 / 7

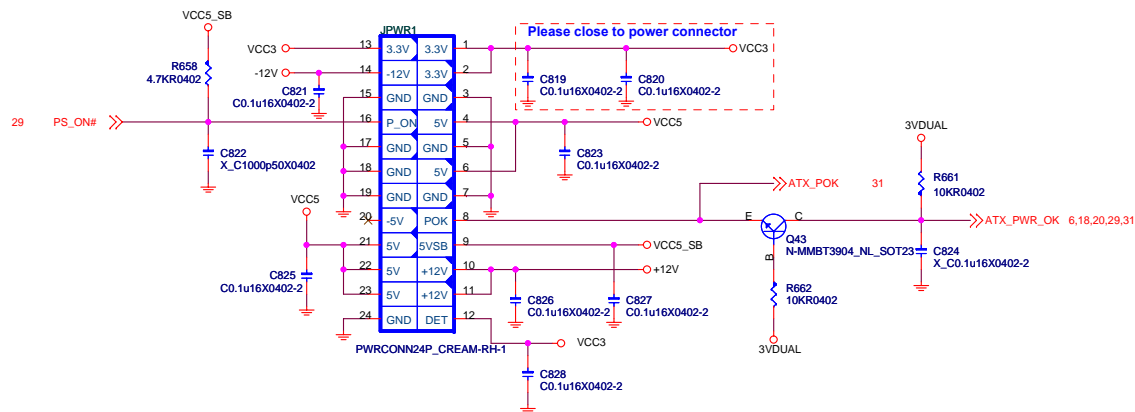


Front Panel USB Connector For USB Port 8 / 9

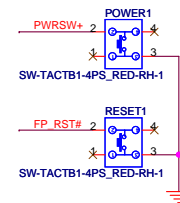


ATX Power Connector / Front Panel / LED

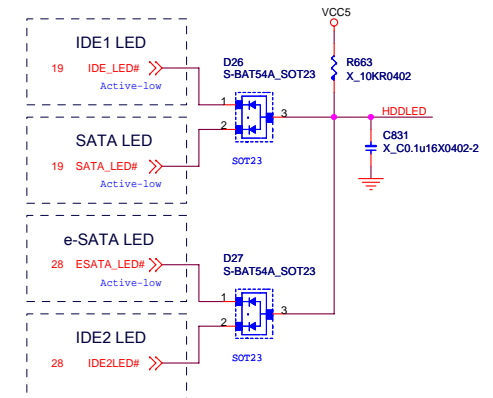
24 Pin ATX Power Connector



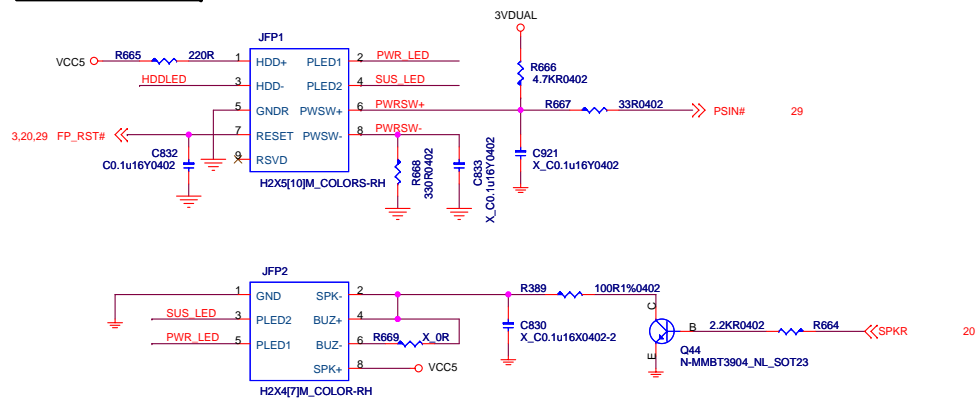
Power and Reset Button



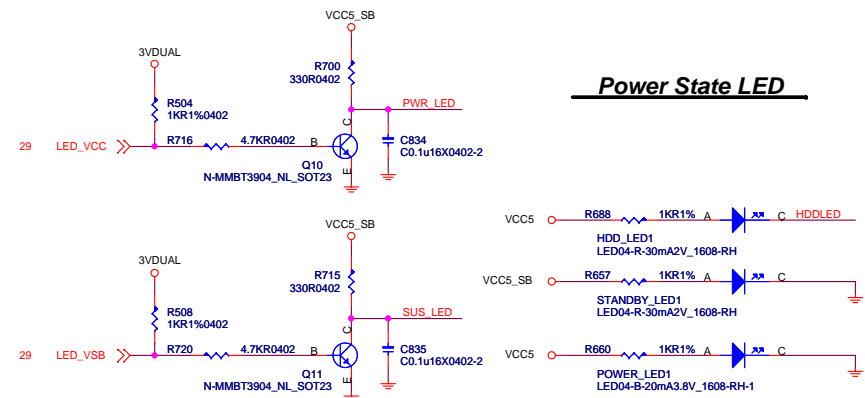
HDD LED

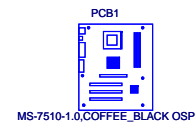
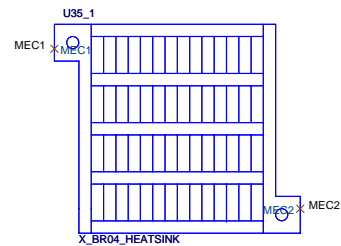
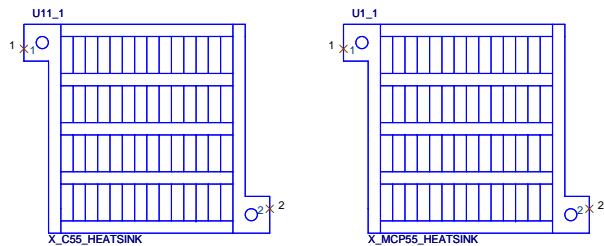


Front Panel

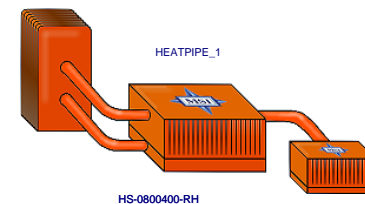


Power State LED



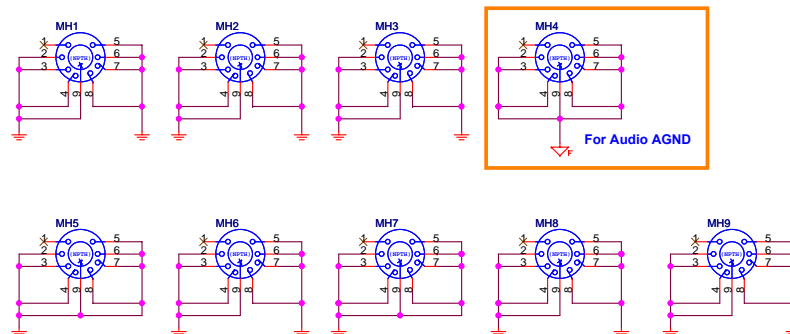
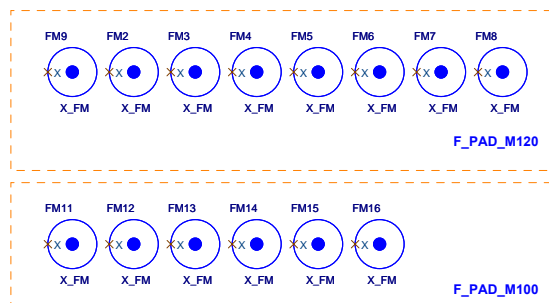


PD0-0751010-D05 (昆源)
PD0-0751010-Y43 (育富)



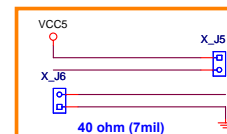
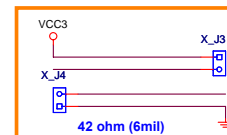
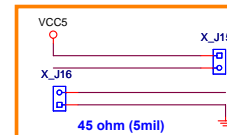
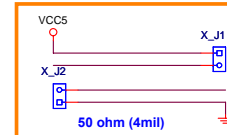
Optics Orientation Holes

PCB Mounting Holes

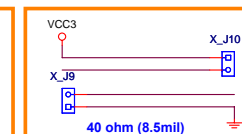
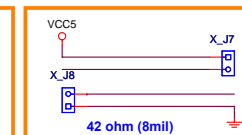
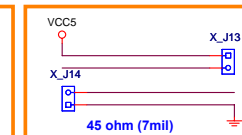
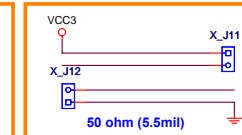


Simulation

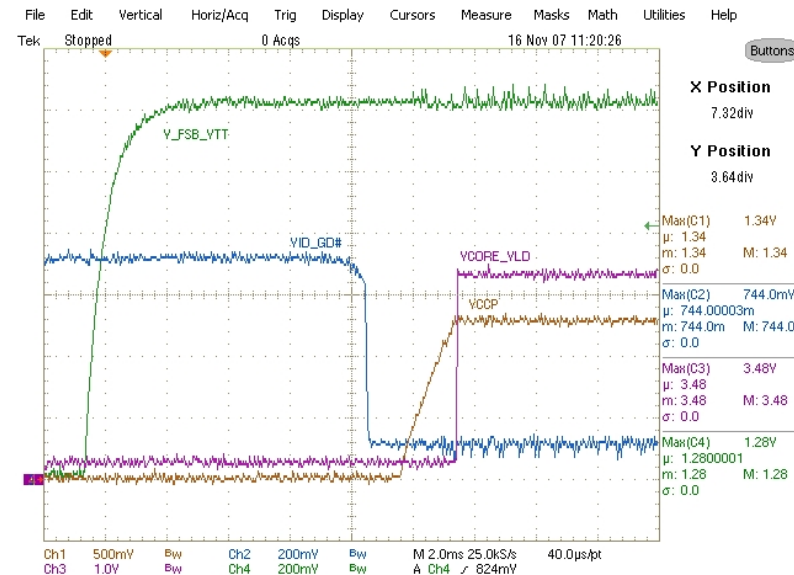
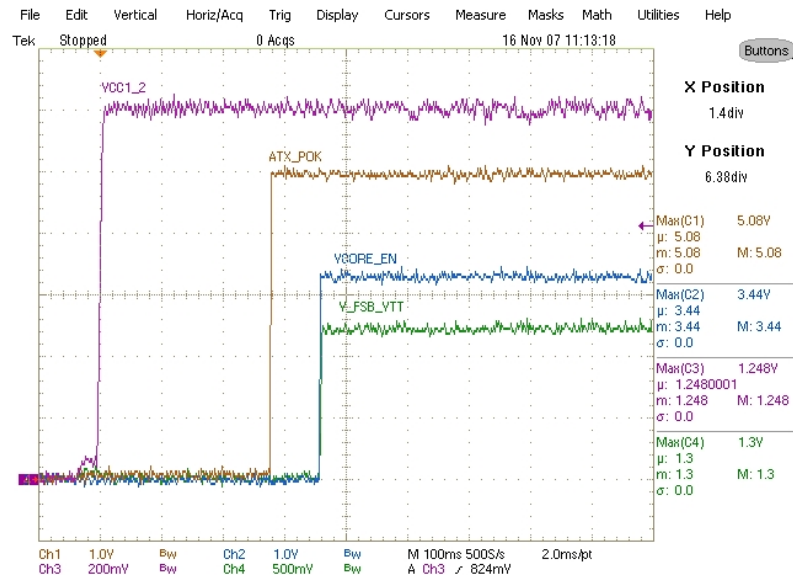
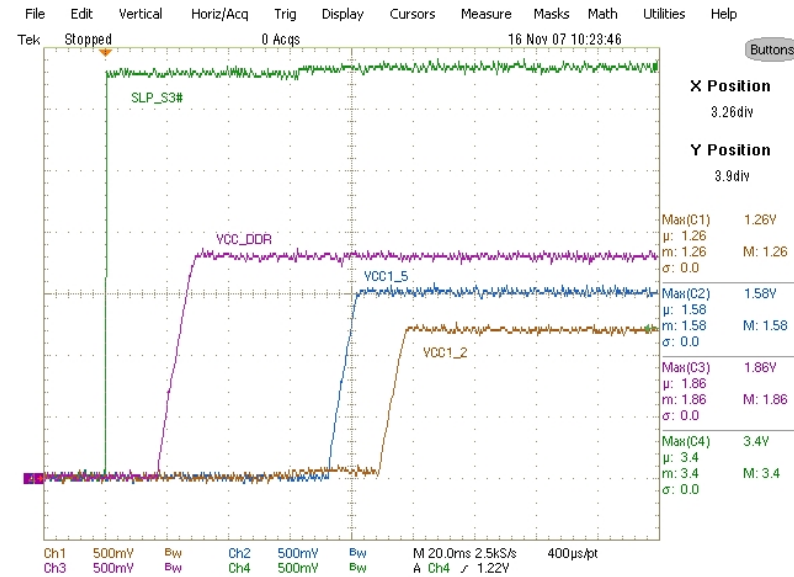
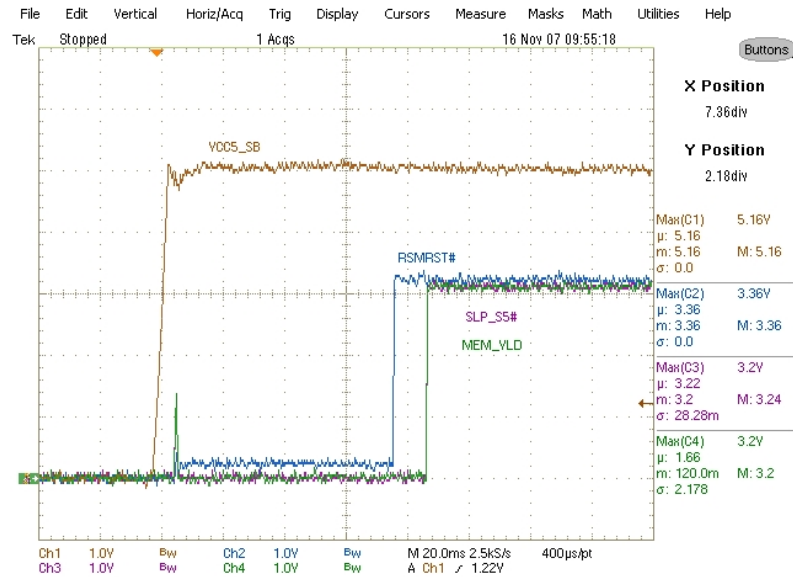
Top and Bottom layer



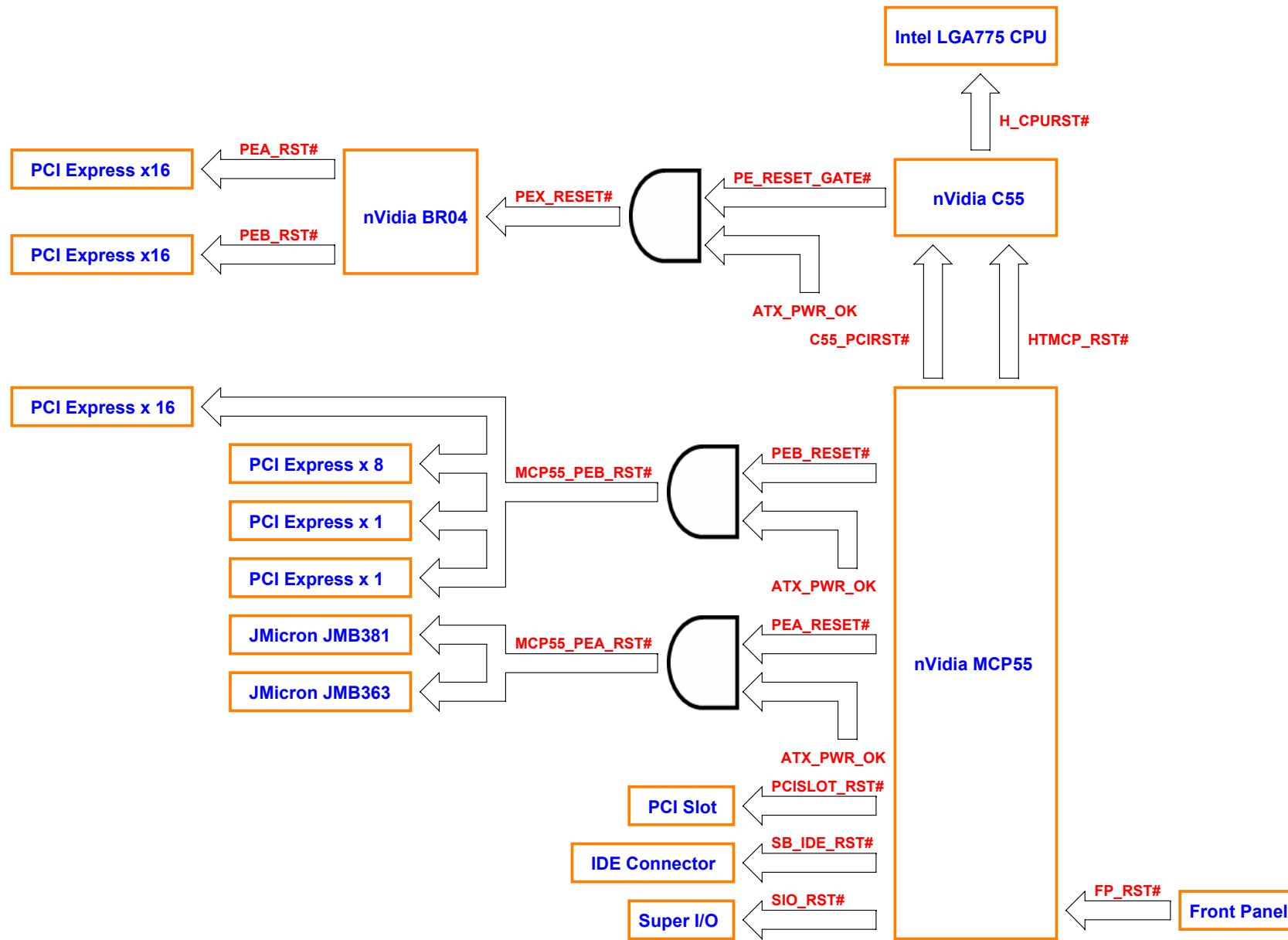
INT1 and INT2 layer



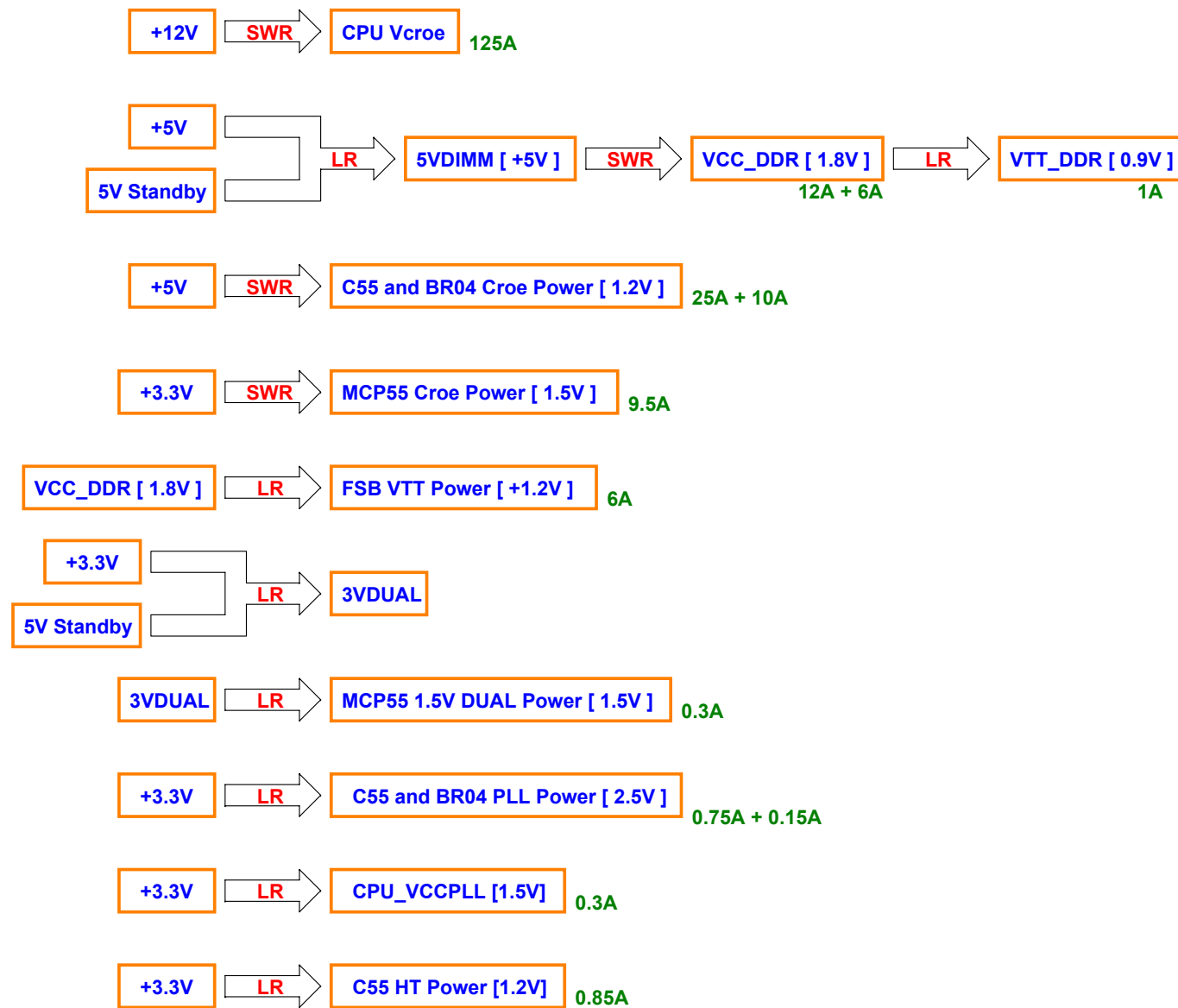
Power On/Off Sequence



System Reset Map



Syatem Power Map



Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCI0REQ# PCI0GNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	BR04
H_CPURST#	CPU
HTMCP_RST#	C55
PE_A_RESET#	BR04 PCI Express x 16 Primary Slot
PE_B_RESET#	BR04 PCI Express x 16 Secondary Slot
PEA_RESET#	JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller
PEB_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot MCP55 PCI Express x 1 Slot
PCISLOT_RST#	MCP55 PCI Slot
C55_PCIRST#	C55
SB_IDE_RST#	Master IDE Connector
SIO_RST#	Super I/O

SuperI/O GPIO Function

Pin Name	Function Description
GP4	CPU_GTL_REF Select
GP5	Reset PWM
SLOT0CC#	Detect CPU remove or not
COPEN#	Detect Case Open or not

MCP55 GPIO Function

Pin Name	Function Description
GP10	USB Connector OC# Detect

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C55 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C55 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C55
PE_BR04_CLK PE_BR04_CLK#	C55 to BR04
BF_PE_CLK BF_PE_CLK#	C55 to Clock Buffer
PE_BR04_REFCLK PE_BR04_REFCLK#	Clock Buffer to BR04
PE_A_REFCLK PE_A_REFCLK#	Clock buffer to Express x 16 Primary Slot
PE_B_REFCLK PE_B_REFCLK#	Clock Buffer to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C55
C55_25MHZ	MCP55 to C55
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to JMicron JMB363 eSATA Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header

2007-07-25
Crate First Version Schematic

2007-08-08
7510-0A Net-in

2007-08-22
Update project Spec.
From PDC42819 change to JMB363

2007-09-07
Update nVidia PCI Express clock jitter issue solution

2007-09-12
Gerber Out

2007-09-25
Assembly

2007-10-01
HW gat sample board

2007-10-16
7510-0B Net-in

Update circuit
1. Change ACPI solution from MS12 to uPI

2007-10-30
7510-0B Gerber Out

2007-11-11
Assembly

2007-11-27
7510-1.0 Net-in

Update circuit
1. Change Fan control solution from PWM Mode to Liner Mode